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RECIRCULATING REMAINDER

When the John Fluke Manufacturing Company entered the digital field it was decided that any instrument that we did manufacture would have to meet our established reputation for accuracy and reliability. Existing techniques of conversion were explored and rejected, either for their inability to meet the accuracy requirements, or their high cost, and/or their failure probability. The problem was solved in our own engineering department with the invention and development of the Recirculating Remainder technique of conversion.

High on our list of requirements, as always, is accuracy, and Recirculating Remainder gave us the accuracy we required, plus a low parts count and the resultant low power requirement for a highly reliable instrument. The technique also gave us excellent linearity and excellent Normal Mode Noise Rejection.

As seen in Figure 1 the first block represents the Input Signal Conditioner. It is the function of this circuitry to convert the input to the instrument to a DC signal within the basic range of the instrument. In the case of DC the usual task is attenuation. For AC it is necessary to convert the AC to DC via rectification and then attenuate the signal. In the case of ohms it is necessary to convert the ohms measurement to voltage within the basic range of the instrument. And with millivolt measurements it is usually necessary to amplify the signal up to the basic input level.

The second block in the system is Polarity Switching. Since we want an automatic instrument, we include Polarity Sensing and Switching as an integral feature. Polarity Sensing and Switching feeds the A - D, or Analog to Digital Amplifier, which is the heart of the instrument. It is an Operational Amplifier with a differential input. In the case of our example circuitry this amplifier has a gain of ten. Through the years the John Fluke Manufacturing Company has made extensive use of the Operational Amplifier to achieve accuracy and stability in our instrumentation. The application in the Recirculating Remainder system is not a particularly difficult one for a good Operational Amplifier. In the example system shown we will consider the basic input to the instrument as zero to 1.2 volts. This would correspond to the 1 volt range with 20% over-ranging. The input to the Polarity Switching circuit would be plus or minus zero to 1.2 volts DC and the output of the polarity switching would always be zero to plus 1.2 volts.

The A to D Amplifier feeds the Analog Comparator. It is the function of the analog comparator to produce current any time the output voltage of the A - D Amplifier is 1 volt or higher. Outputs of less than 1 volt from the Amplifier will result in no current from the Analog Comparator. Current from the Analog Comparator feeds the Oscillator. It is the function of the Oscillator to produce a train of pulses whenever it is fed current from the Analog Comparator.

The pulse train generated by the Oscillator is counted by the BCD Counter. The counting is done in BCD, or Binary Coded Decimal format, as shown in Figure 2. This counter is reset to zero after each digitizing period.

One of the circuits that is fed by the BCD Counter is the Primary Ladder. This Ladder generates 0.1 volt output for every pulse that is translated by the Counter. Should the Oscillator produce six pulses the output of the BCD Counter would be a BCD 6 and the output of the Ladder would be 0.6 volts. The output of the Ladder is fed back to the input of the A to D Amplifier.

It should be noted that one input of the differential A to D Amplifier is from the Polarity Switching circuit, and the other is from the Primary Ladder. It is characteristic of a differential amplifier that when the inputs to the amplifier are equal, the output will be zero. The output voltage of a Differential Amplifier is equal to the difference voltage input, times the gain of the amplifier. (See Figure 3.)

The BCD Counter also feeds the Display. As numbers are digitized in Recirculating Remainder they are sequentially displayed. In orther words, the numbers blink ON in sequence. The hundreds digit turns ON and

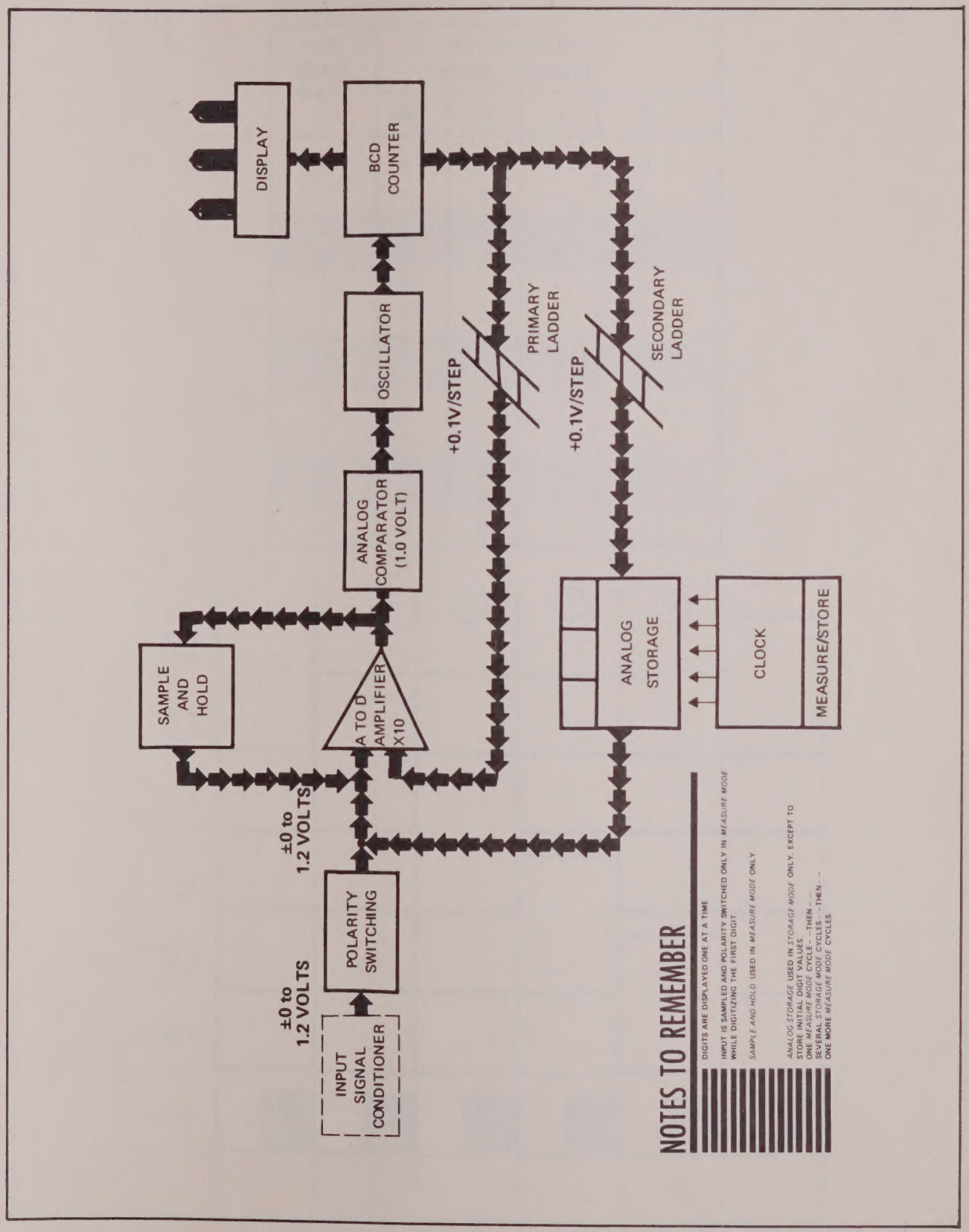

DISPLAY
BCD COUNTER
OSCILLATOR
ANALOG COMPARATOR (1.0 VOLT)
SAMPLE AND HOLD
A TO D AMPLIFIER X10
+0.1V/STEP
PRIMARY LADDER
+0.1V/STEP
SECONDARY LADDER
ANALOG STORAGE
CLOCK
MEASURE/STORE
±0 to 1.2 VOLTS
POLARITY SWITCHING
±0 to 1.2 VOLTS
INPUT SIGNAL CONDITIONER
NOTES TO REMEMBER
DIGITS ARE DISPLAYED ONE AT A TIME
INPUT IS SAMPLED AND POLARITY SWITCHED ONLY IN MEASURE MODE WHILE DIGITIZING THE FIRST DIGIT.
SAMPLE AND HOLD USED IN MEASURE MODE ONLY.
ANALOG STORAGE USED IN STORAGE MODE ONLY, EXCEPT TO STORE INITIAL DIGIT VALUES -- THEN -- ONE MEASURE MODE CYCLE -- THEN -- SEVERAL STORAGE MODE CYCLES -- THEN -- ONE MORE MEASURE MODE CYCLES.

FIGURE 1.

CCO PULSE COUNT	SIXTEEN–STATE BINARY COUNTER			
	6Z	6Y	7X	7W
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1

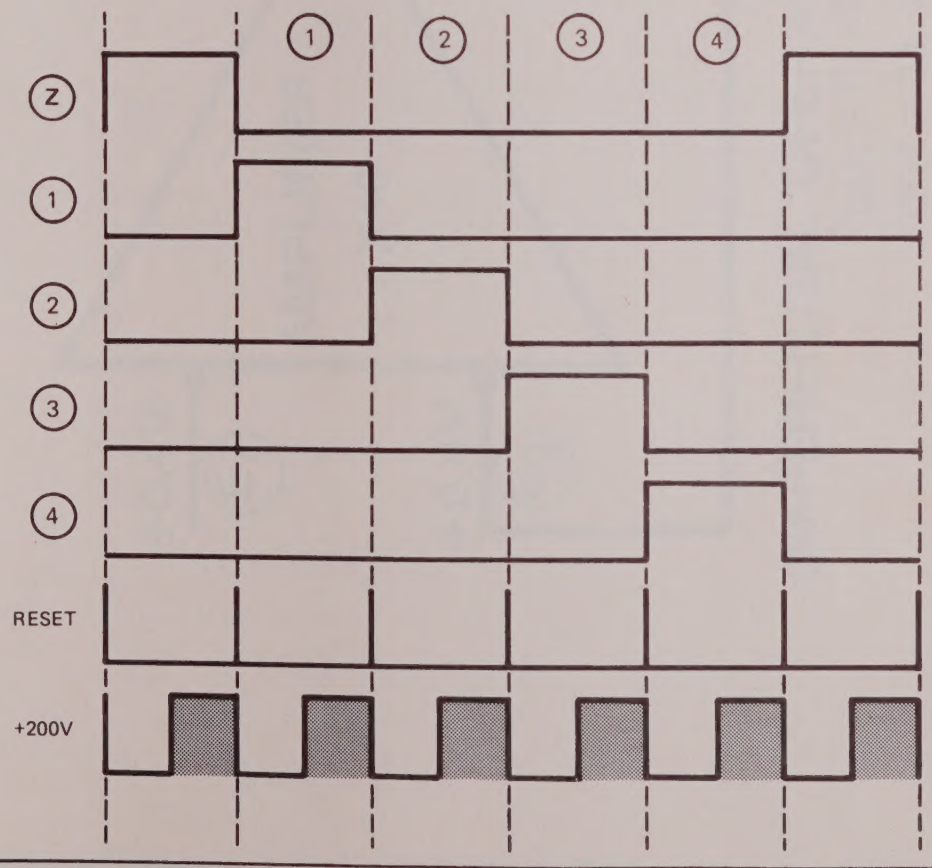
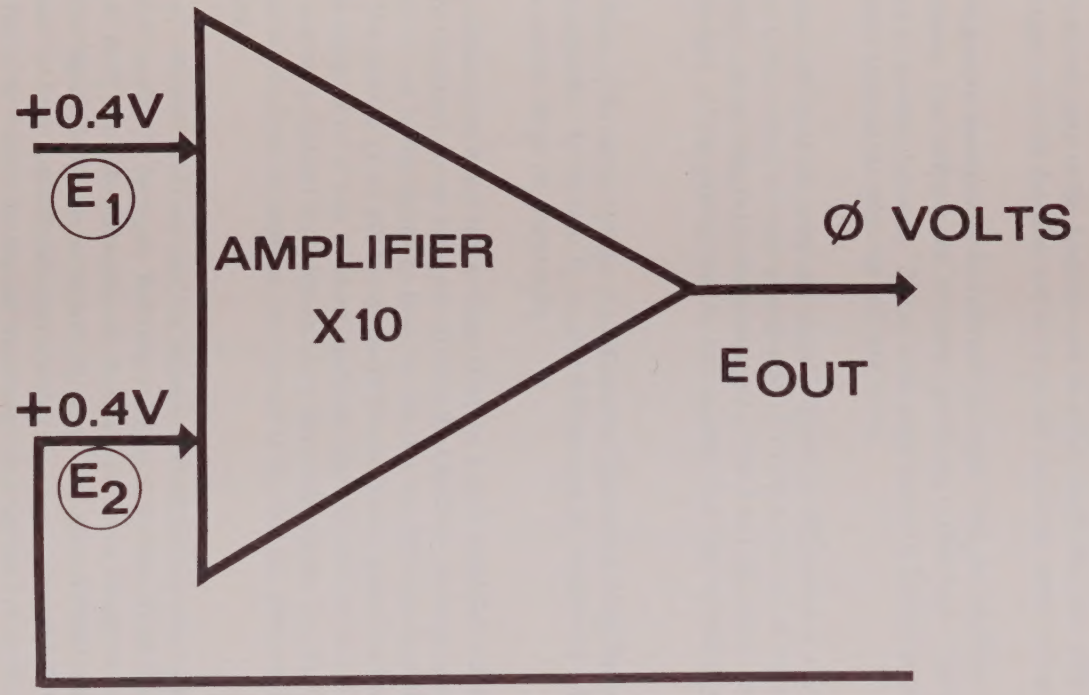


FIGURE 2.



DIFFERENTIAL OPERATIONAL AMPLIFIER

$E_{OUT} = E_1 - E_2 \times GAIN$

$E_{OUT} = 0.4 - 0.4 \times GAIN = \emptyset$ VOLTS

FIGURE 3.

displays the number that was digitized, then turns OFF. The tens digit turns ON and displays the number that was digitized, then turns OFF. The ones digit turns ON, displays the number that was digitized, turns OFF, etc. Applying −40 volts DC at the input to the Block Diagram shown in Figure 4, the Input Signal Conditioner would attenuate the forty volts down to −0.4 volts by dividing by 100. The −0.4 volts would be fed to the Polarity Switching Circuitry. The Polarity Switching Circuit will sense the negative voltage and cause FET transistor switches to operate in such a manner as to apply the +0.4 volts to the A to D Amplifier.

With +0.4 volts on one input to the Amplifier and the other input being zero volts from the Primary Ladder the resultant voltage out of the Amplifier will be +4.0 volts due to the times ten gain of the Amplifier.

The Analog Comparator sensing more than one volt of output from the Amplifier produces current which is fed to the Oscillator. The Oscillator will commence producing a pulse train. It is interesting to note that the rate of pulsing is a function of current. That is, when more current is fed to the Oscillator the faster it will pulse. As the current is reduced the pulse rate will slow down.

The BCD Counter will count the pulses and translate them into BCD notation as shown. The BCD output is fed to the Primary Ladder which will have an output of +0.4 volts at the end of the fourth pulse. The +0.4 volt from the Primary Ladder being fed to the lower input of the A to D Amplifier, the upper input of the A to D Amplifier is +0.4 volts. At this point in time we have applied +0.4 volts to both inputs of the differential A to D Amplifier.

As shown in Figure 3, the output voltage of a Differential Operational Amplifier is equal to E_1 minus E_2 times the gain of the amplifier. In this case, E_1 equals +0.4 volts and E_2 equals +0.4 volts, the difference being zero volts and the output, times 10, is zero volts.

The Analog Comparator no longer sees a voltage from the A to D Amplifier and, therefore, no longer produces current for the Oscillator; current being cut off from the Oscillator, no more pulses will be produced. The circuitry is in a state of rest, having digitized a four. At this time the BCD four from the Counter is fed to the Display circuitry. The Decoder Driver will decode the BCD four, place a ground on the "4" line to the display tubes. During this initial period of time the most significant digit tube will be ionized, but only for a few milliseconds. As each number is digitized in the Recirculating Remainder system it is displayed for a short time only. The numbers are displayed in sequence, but at a rate so fast that the persistency of the human eye does not see the blinking.

The example of −40 volts works out well, but we were working with an even voltage. Let us take the example of 42.31 volts AC applied to the input. Referring to Figure 5, the first action that must take place is the conversion of the AC to DC, then the attenuation of the result down to a voltage within the basic range of the instrument; the Input Signal Conditioner serves both purposes. The AC is rectified and attenuated so that the resultant output from the Input Signal Conditioner is within the range of zero to 1.2 volts, or, in this case, +.4231 volts, which is fed to the Polarity Sensing and Switching circuit and then on to the input to the A to D Amplifier. In order to digitize the first significant digit the output of the A to D Amplifier will be 4.231 volts until the Analog Comparator has supplied current to the Oscillator long enough for four fulses to be generated, which are counted by the BCD Counter. The output of the Primary Ladder is now 0.4 volts, and the inputs to the A to D Amplifier are +0.4 volts and +0.4231 volts, the difference being +0.231 volts. The output of the amplifier will be +0.231 volts, insufficient to cause the Analog Comparator to supply further current to the Oscillator. The Display Circuit will display a 4 in the first tube. All of the other display tubes will be dark. The output of the A to D Amplifier after the fourth pulse has been counted will be +0.231 volts, which is the remainder voltage. Instrument timing will cause the Sample and Hold circuit to accept the 0.231 volts into a storage capacitor where it will be stored until we need it to digitize the next increment of voltage. The Clock will also reset the BCD Counter to zero. It is the Clock that synchronizes the Display to operate in the proper sequence and at the proper time.

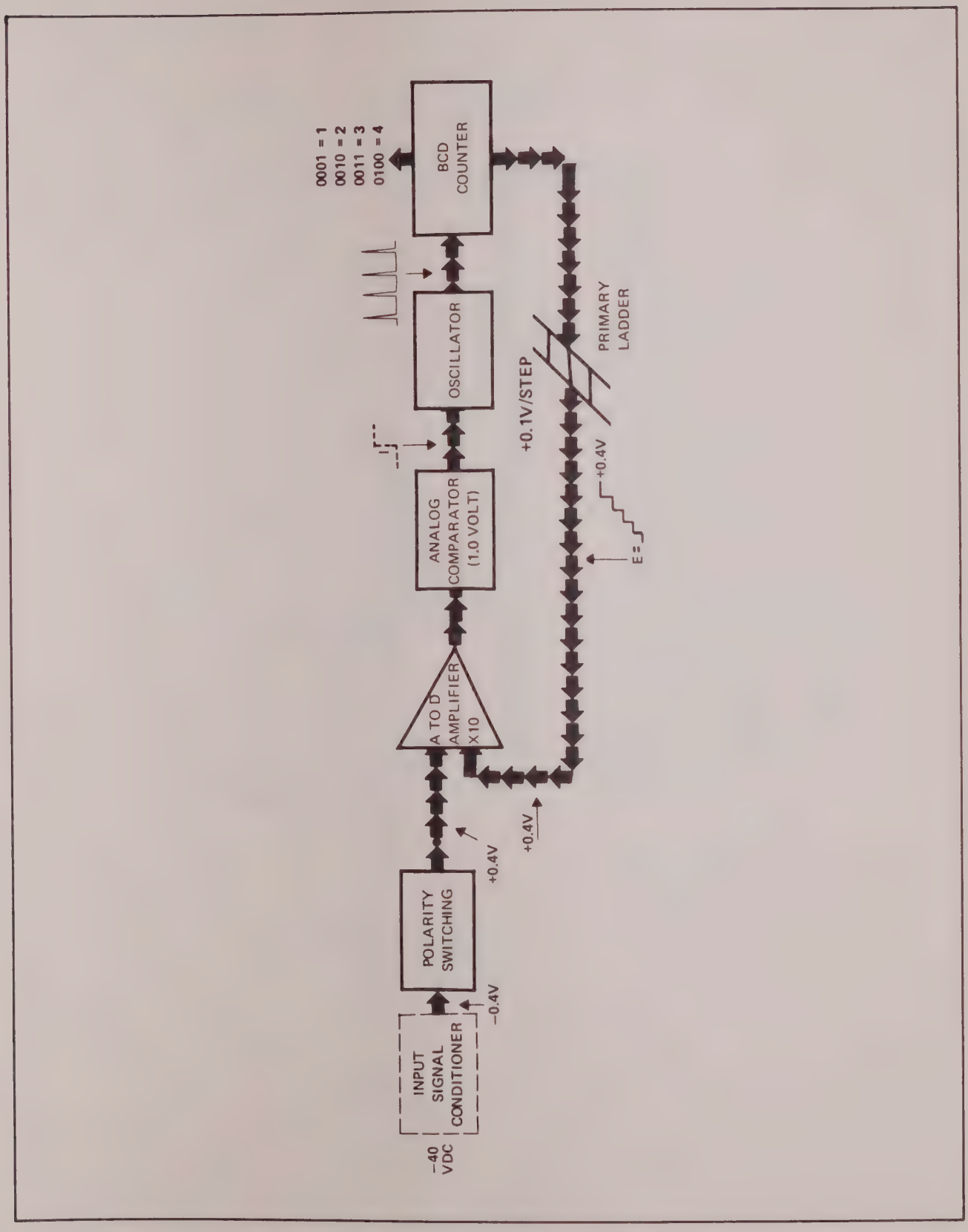

0001 = 1
0010 = 2
0011 = 3
0100 = 4
BCD COUNTER
OSCILLATOR
ANALOG COMPARATOR (1.0 VOLT)
A TO D AMPLIFIER X10
POLARITY SWITCHING
INPUT SIGNAL CONDITIONER
−40 VDC
−0.4V
+0.4V
+0.4V
+0.1V/STEP
PRIMARY LADDER
+0.4V
E=

FIGURE 4.

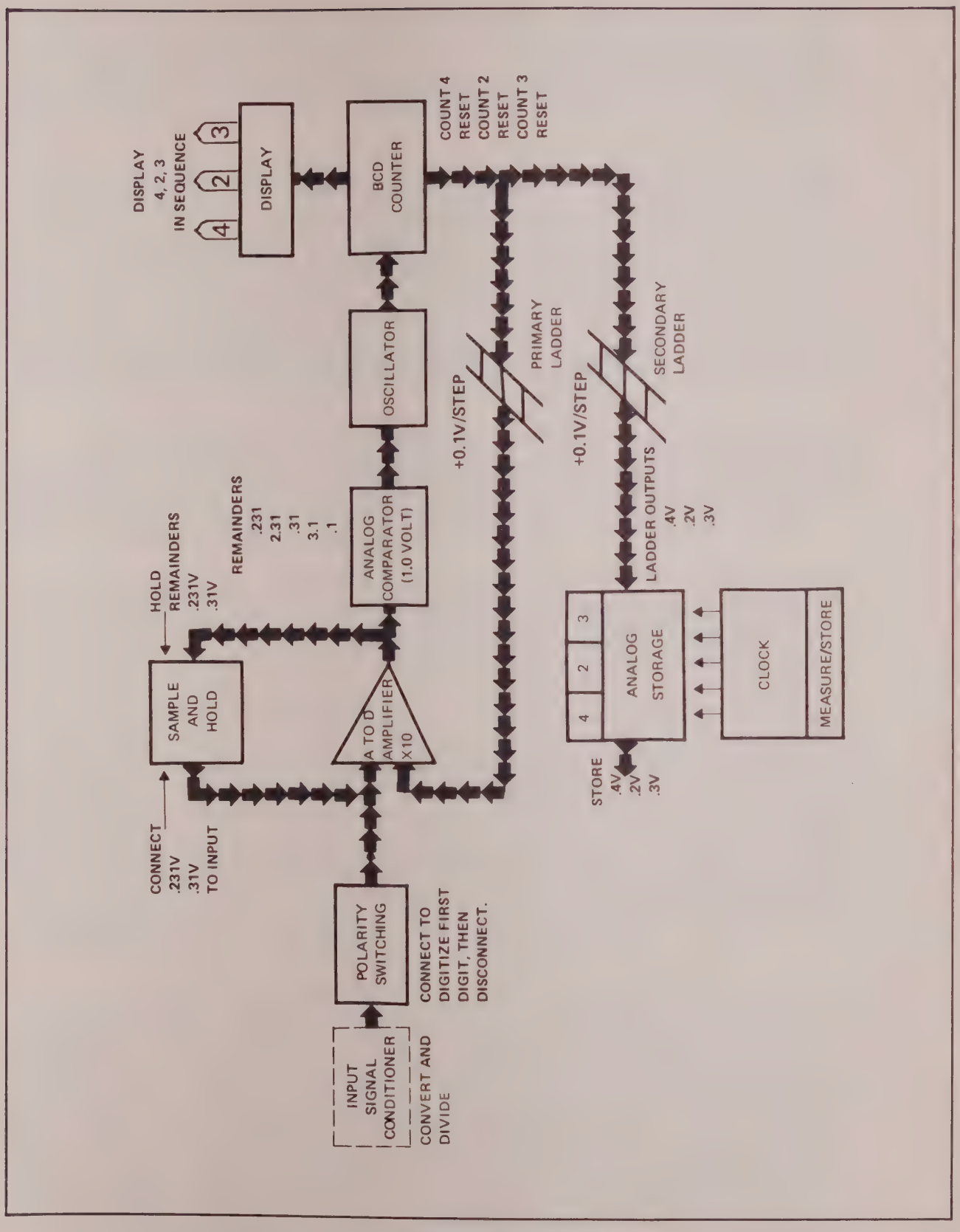

DISPLAY
4, 2, 3
IN SEQUENCE
4
2
3
DISPLAY
BCD
COUNTER
COUNT 4
RESET
COUNT 2
RESET
COUNT 3
RESET
OSCILLATOR
PRIMARY
LADDER
SECONDARY
LADDER
+0.1V/STEP
+0.1V/STEP
HOLD
REMAINDERS
.231V
.31V
REMAINDERS
.231
2.31
.31
3.1
.1
ANALOG
COMPARATOR
(1.0 VOLT)
LADDER OUTPUTS
.4V
.2V
.3V
SAMPLE
AND
HOLD
A TO D
AMPLIFIER
X10
4
2
3
ANALOG
STORAGE
CLOCK
MEASURE/STORE
STORE
.4V
.2V
.3V
CONNECT
.231V
.31V
TO INPUT
POLARITY
SWITCHING
CONNECT TO
DIGITIZE FIRST
DIGIT, THEN
DISCONNECT.
INPUT
SIGNAL
CONDITIONER
CONVERT AND
DIVIDE

FIGURE 5.

At the next moment in time the Clock will cause the input line to the Sample and Hold circuit to cut OFF, while turning the output line from the Sample and Hold circuit ON and connecting it to the input to the A to D Amplifier. (See Figure 5.) This action causes the 0.231 volts that was stored in the Sample and Hold circuit to be applied to the Amplifier input. The input from the primary ladder is once again zero volts, having been reset as a result of the counter reset that was applied during the last Clock action in the first digitizing period.

The voltage from the Amplifier will be 2.31 volts. With more than 1 volt output from the Amplifier the Analog Comparator will once again supply current to the Oscillator. The Oscillator Pulses will be counted and translated to BCD output by the BCD Counter. Remember that the Clock had caused the BCD Counter to be reset to zero during the previous time period. When the Counter was reset the Display Tube was extinguished and now all of the display tubes are dark. When the oscillator has pulsed twice the output of the Primary Ladder will be .2 volts, which is fed back to the input of the A to D Amplifier. Figure 5 shows an additional Ladder connection to the output of the Counter. A Secondary Ladder has simultaneous outputs with the Primary Ladder. These output voltages are fed to a circuit called Analog Storage. When the 4 was digitized in the first period the output of the Secondary Ladder was +0.4 volts; the Clock will cause the 0.4 volts to be stored in Analog Storage in a specific location reserved for the first digit.

The circuit has just digitized the 2 and now the Clock will cause the +0.2 volts from the Secondary Ladder to be stored in Analog Storage in a position reserved for the second digit. +0.2 volts being fed back to the input of the A to D Amplifier from the Primary Ladder caused the input voltage difference to the Amplifier to be .031 volts, and the output of the Amplifier to be 0.31 volts, which is less than one volt. Consequently, the Analog Comparator will no longer supply current.

A "2" having been digitized, BCD information is fed to the Display circuit where the "2" is displayed as the second most significant digit. The remainder voltage from the Amplifier, which was .31 volts, will be stored in the Sample and Hold circuit. At this moment in time the Display tube will be extinguished and the BCD Counter will be reset to zero which causes the output voltage of the Ladders to be reduced to zero volts.

The output of the Sample and Hold will cause the .31 volts just stored to be applied to the input of the A to D Amplifier . . . resulting in an output of 3.1 volts. The Analog Comparator will produce current, the Oscillator will start generating a pulse train. The Counter will count that pulse train and the BCD Counter will translate those pulses into BCD format, causing each Ladder to increase its output by 0.1 volt per pulse. At the end of the third pulse the inputs to the A to D Amplifier are +0.3 volts from the Primary Ladder, and .31 volts from the Sample and Hold circuit, where a difference voltage of .01 times 10 will result in an output of 0.1 volt, which is insufficient to cause the Analog Comparator to supply further current. "3" having been digitized, the BCD Counter will now place a ground on the "3" line to all of the display tubes, so that the "3" will be caused to display in the least significant digit display device. The Secondary Ladder's output will be 0.3 volts, which is fed to Analog Storage where it is stored in a capacitor reserved for the third digit storage.

In summary, during the first digitizing timer period, the input to be measured was sampled and the most significant number was digitized and displayed. Its remainder was stored in Sample and Hold, and an analog value representative of the first digit magnitude was stored in Analog Storage. The Polarity Switch then disconnected the input from the instrument. The Counters were reset and the remainder voltage from Sample and Hold was connected to the input of the A to D Amplifier. Once again the instrument digitizes the second digit, displays the second digit, stores a value in Analog Storage that corresponds to the magnitude of the second digit, and stores the remainder in Sample and Hold. The Counter is reset and Sample and Hold is connected to the input of the A to D Amplifier and the last digit is digitized, displayed, and a value representative of the magnitude of the third digit is stored in Analog Storage. Since in the example given we were using a three digit voltmeter, the digitizing process is completed, and through we had a .1 volt remainder there was no place left to store it. This completes the MEASURE MODE of Operation.

STORAGE MODE

Recirculating Remainder instruments operate in two modes of operation - Measurement Mode and Storage Mode. It is interesting to note that during Measurement Mode, Recirculating Remainder stores analog voltages in Analog Storage, but they are never used in the Measurement Mode.

Taking the instrument into Storage Mode, the Sample and Hold circuit will not be used, and during the first time period the analog value stored in Analog Storage most significant digit position is connected to the input of the A to D Amplifier, and the digit is digitized and displayed and the Secondary Ladder replaces the value in Analog Storage. (See Figure 6.) Each digit is digitized in turn using the values that were stored in Analog Storage. Each time a digit is digitized as one of the final actions in that time period, the output of the Secondary Ladder restores the analog value in Analog Storage.

Depending upon the Sample Rate in Recirculating Remainder, it is customary for an instrument to operate in one measurement mode cycle and then six to eighteen storage mode cycles. In some cases where instruments are made for specific interface into systems such as the 8200, the 8300 and the 8400, instruments can be operated in a continuous measurement mode.

In summary, there are two modes of operation - Measurement Mode and Storage Mode. In the usual application an instrument proceeds through one Measurement Mode of operation and then several cycles of Storage Mode.

MEASUREMENT MODE (Refer to Figure 7)

Review and Highlight Time

There are several significant points that we must remember in order to understand Recirculating Remainder. There are two modes of operation - Measure Mode and Storage Mode. In the usual application, an instrument proceeds through one Measurement Mode of operation and then several cycles of Storage Mode.

A Review of the Actions in Measurement Mode.

MEASURE MODE

a. The input is sampled.

b. The first digit is digitized and displayed.

c. The input is disconnected by the Polarity Switch.

d. The remainder of the first digit is stored in Sample and Hold.

e. An analog value is stored in Analog Storage for later use in the Storage Mode.

f. The Counter is reset.

g. The remainder voltage that was stored in Sample and Hold is connected to the input of the A to D Amplifier.

h. The second digit is digitized and displayed.

i. The remainder is stored in Sample and Hold.

j. An analog value is stored in the second digit position in Analog Storage.

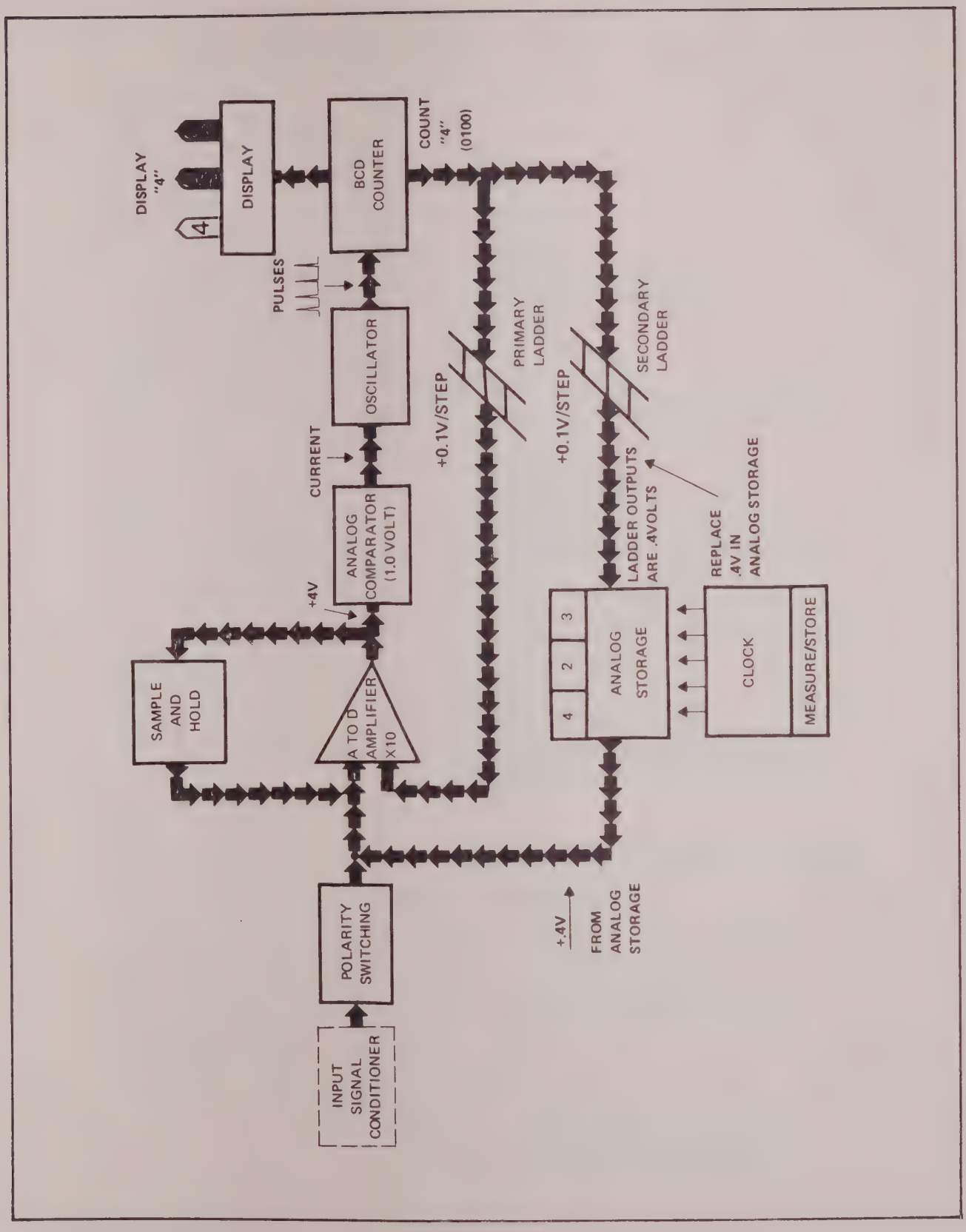
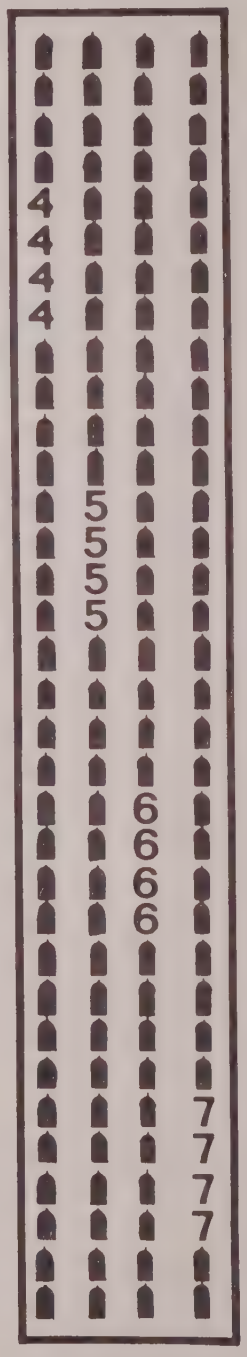

DISPLAY "4"
DISPLAY
BCD COUNTER
COUNT "4" (0100)
PULSES
OSCILLATOR
CURRENT
ANALOG COMPARATOR (1.0 VOLT)
+4V
+0.1V/STEP
PRIMARY LADDER
+0.1V/STEP
SECONDARY LADDER
LADDER OUTPUTS ARE .4VOLTS
REPLACE .4V IN ANALOG STORAGE
SAMPLE AND HOLD
A TO D AMPLIFIER X10
4
2
3
ANALOG STORAGE
CLOCK
MEASURE/STORE
+.4V
FROM ANALOG STORAGE
POLARITY SWITCHING
INPUT SIGNAL CONDITIONER

FIGURE 6.

MEASURE MODE



Z — Internal error correction. (Offset removal)
1 — Sample input
1 — Sense and switch polarity
1 — Digitize first digit
1 — Display first digit
1 — Store remainder in Sample and Hold
1 — Store analog value in Analog Storage
1 — Disconnect input
1 — Display OUT
1 — Reset Counter
2 — Connect remainder from Sample and Hold to A/D Amplifier
2 — Digitize second digit
2 — Display second digit
2 — Store remainder in Sample and Hold
2 — Store analog value in Analog Storage
2 — Disconnect Sample and Hold from A/D Amp. input
2 — Display OUT
2 — Reset Counter
3 — Connect remainder from Sample and Hold to A/D Amp.
3 — Digitize third digit
3 — Display third digit
3 — Store remainder in Sample and Hold
3 — Store analog value in Analog Storage
3 — Disconnect Sample and Hold from A/D Amp. input
3 — Display OUT
3 — Reset Counter
4 — Connect remainder from Sample and Hold to A/D Amp
4 — Digitize fourth digit
4 — Display fourth digit
4 — If the fourth is the last digit, ignore any remainder
4 — Store analog value in Analog Storage
4 — Disconnect Sample and Hold from A/D Amp. input
4 — Display OUT
4 — Reset Counter

NOTE: Depending on the state of the Measure Store Multivibrator the instrument will return to "Z" time in either Measure Mode (unusual case) or enter Storage Mode.

FIGURE 7.

k. The Counter is reset.

l. The remainder from the second digit is connected to the A to D Amplifier and is digitized and displayed. This being the third and last digit the instrument is ready to proceed into Storage Mode.

NOTE!

After digitizing the last digit all three digits have been stored in Analog Storage, and at this point in time, the Measure Store portion of the clock causes the instrument to shift to Storage Mode of operation.

A Review of Actions in Storage Mode

STORAGE MODE (Refer to Figure 8)

a. The first analog quantity from Analog Storage is applied to the A to D Amplifier and digitized.

b. The first digit is displayed.

c. Analog quantity is restored in Analog Storage.

d. The display is extinguished and the Counter reset.

e. The second digit is applied to the input of the A to D Amplifier from Analog Storage and digitized.

f. The second digit is displayed.

g. The second digit quantity is restored in Analog Storage.

h. The display goes out and the Counter is reset.

i. The third digit quantity from Analog Storage is applied to the input of the A to D Amplifier and digitized.

j. Third digit is displayed.

k. Third digit quantity is replaced in Analog Storage.

l. The display goes out and the Counter is reset, and the instrument is ready to start another cycle of either Storage Mode or Measurement Mode.

SCHEMATIC DIAGRAM DESCRIPTION

A TO D CONVERTER (Refer to Figure 9 and 10)

It has been demonstrated in the Block Diagram description that the Recirculating Remainder conversion process is synchronously operated. A Ring Counter fed by an internal Clock develops the time periods required. In our schematic example, the Ring Counter develops five time periods of 4 milliseconds each. The ZERO time period and four remaining periods identified as "1' , "2", "3" and "4". Our example schematic has been stripped of all circuits that are not essential to the description of the conversion process and does not include any of the refinements necessary for an accurate instrument.

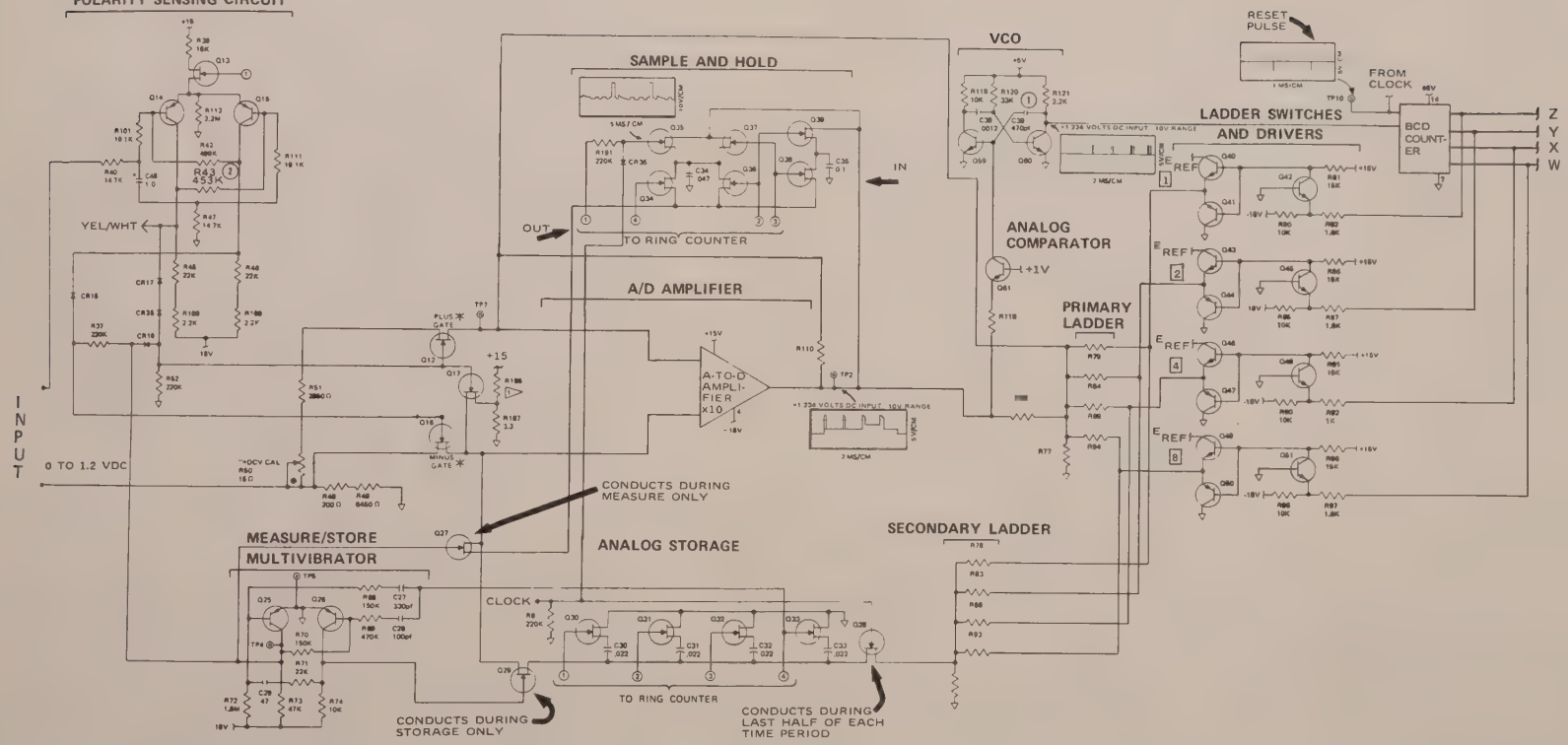

POLARITY SENSING CIRCUIT
YEL/WHT
INPUT
0 TO 1.2 VDC
SAMPLE AND HOLD
OUT
TO RING COUNTER
IN
A/D AMPLIFIER
A-TO-D AMPLIFIER X10
CONDUCTS DURING MEASURE ONLY
MEASURE/STORE MULTIVIBRATOR
ANALOG STORAGE
CLOCK
TO RING COUNTER
CONDUCTS DURING STORAGE ONLY
CONDUCTS DURING LAST HALF OF EACH TIME PERIOD
VCO
RESET PULSE
FROM CLOCK
LADDER SWITCHES AND DRIVERS
BCD COUNTER
Z
Y
X
W
ANALOG COMPARATOR
+1V
PRIMARY LADDER
SECONDARY LADDER
REF

FIGURE 9.

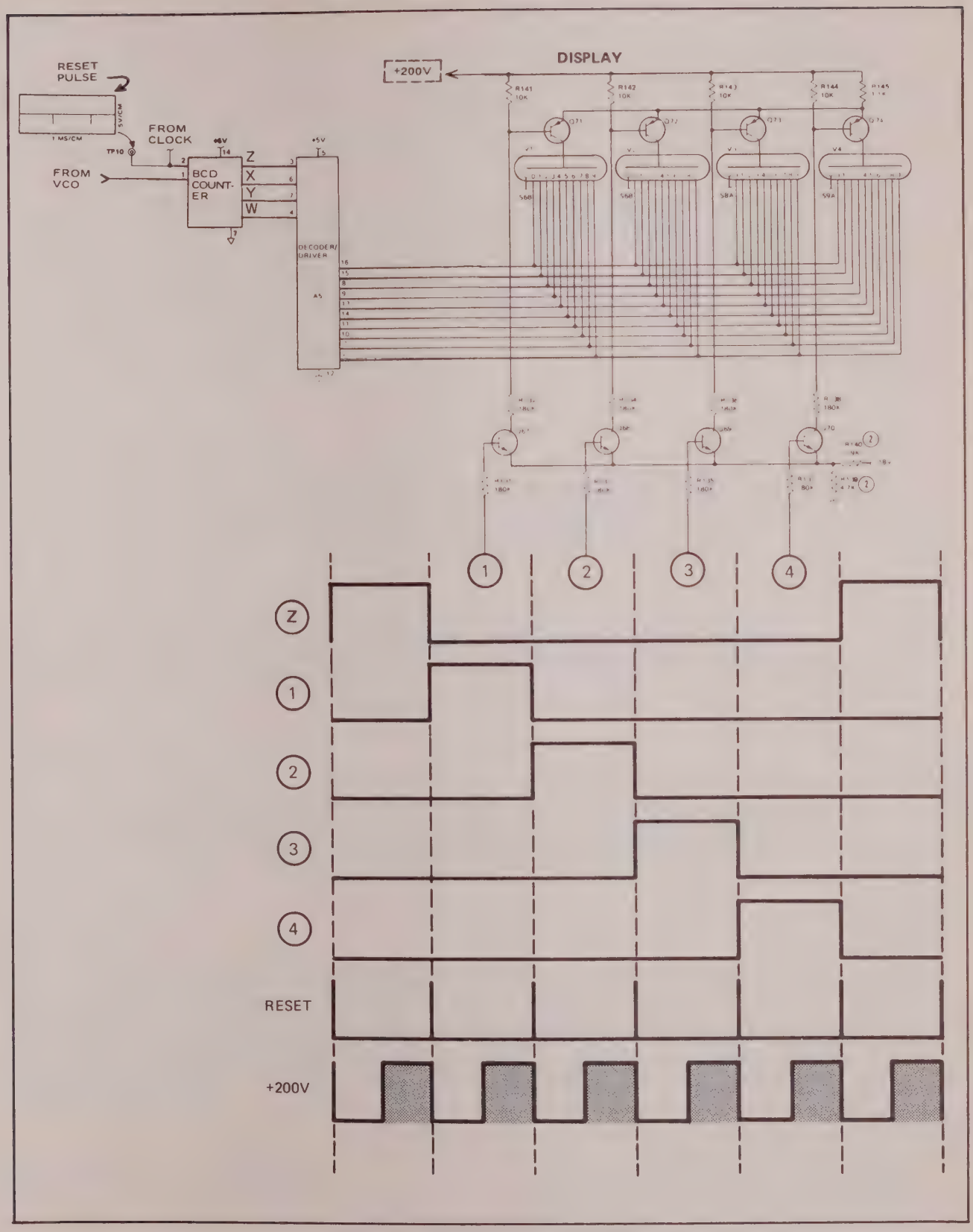

RESET
PULSE
1 MS/CM
5V/CM
TP10
FROM
CLOCK
FROM
VCO
BCD
COUNT-
ER
+6V
+5V
Z
X
Y
W
DECODER/
DRIVER
A5
DISPLAY
+200V
R141
10K
R142
10K
R143
10K
R144
10K
R145
Q71
Q72
Q73
Q74
V1
V2
V3
V4
S6B
S6B
S8A
S9A
1
2
3
4
Z
1
2
3
4
RESET
+200V

FIGURE 10.

POLARITY SENSING CIRCUIT (Figure 9)

The Polarity Sensing Circuit is composed of Q13, Q14 and Q15 and their associated parts. Input from the Input Signal Conditioner arrives at R40. The "1" time period pulse is connected to the Gate of Q13 and enables it only when the instrument is in the "1" time period. The Measure Pulse arriving at the junction of R37 and CR16 enables Q14 and Q15. It is apparent that the Polarity Sensing Circuit is only functional when the instrument is in the "1" time period AND in the Measure Mode of operation.

If the voltage arriving at R40 is negative, Q14 will conduct. This will cause Q12 and Q17 to conduct and apply the input from "+ DCV CAL" R50 to be applied to the input to the A - D Amplifier. Q17 is used to correct the polarity reversal error into the A - D Amplifier. The reason that a negative voltage at R40 causes the "PLUS GATE" to operate, rather than the "MINUS GATE" is due to the fact that the Input Signal Conditioner inverts the input voltage. (A plus voltage into the instrument will arrive at the Polarity Sensing Circuit as a minus voltage.)

Should the voltage arriving at R40 be positive, Q15 will conduct and cause the "MINUS GATE" Q16 to conduct.

A/D AMPLIFIER

The A/D Amplifier is a monolithic, differential amplifier, in an operational amplifier configuration with a gain of 10. In instrument applications, this amplifier has been refined with circuits to make temperature corrections, fast feedback networks to prevent saturation and a variety of other refinements.

ANALOG COMPARATOR

Q61 is connected to the output of the A/D Amplifier, with its Base connected to 1.0 volt reference. When the Emitter voltage exceeds 1.0 volt the transistor will conduct and supply voltage to the Voltage Controlled Oscillator of VCO. The greater the voltage on the Emitter, the greater will be the source power for the VCO.

VCO (Voltage Controlled Oscillator)

The VCO is a multivibrator formed by Q59 and Q60. It has no output until supplied voltage by the Analog Comparator. The pulse repetition rate of the VCO is proportional to the voltage magnitude being fed to it. The greater the voltage, the higher the pulse rate. The output of the VCO is fed to the Counter.

BCD COUNTER

The BCD Counter is an in-line logic pack counter. It is note-worthy that the BCD Counters used in FLUKE instruments are of a variety that are sixteen state counters. This makes it impossible to replace them with the normal "garden variety" counters with ten states. The counter translates the pulses from the VCO into BCD or Binary Coded Decimal format. Refering to Figure 10, the Reset Pulse, which occurs at the end of each time period can be seen. The BCD output of the Counter is fed to the Ladder Switches and Drivers. The BCD output also feeds the Display circuit.

LADDER SWITCHES AND DRIVERS

The output of the 16 state BCD Counter is fed to transistors Q40 through Q51. The output of the ladder switches is applied to both the Primary Ladder and the Secondary Ladder. Each Ladder comprises a

4-bit, weighted-resistor, digital to analog converter. The output of each of the ladders is 0.1 volt per pulse counted, the format of the Ladders is binary 1248. The Primary Ladder feeds the A/D Amplifier input to balance the input to the differential amplifier. The output of the Secondary Ladder feeds analog voltages to the Analog Storage circuit, to be stored for use in the Storage Mode of operation.

ANALOG STORAGE

Each capacitor in the Analog Storage circuit stores an analog voltage that represents the digit developed in each particular time period. For example: C31 stores an analog value that will cause the circuitry to digitize the number that was developed in the second digitizing time period of the last Measure Mode. Q28 conducts during the last half of every time period (after digitizing has been accomplished in that time period). Q30 through Q33 conduct during the time period pulse connected to their respective GATES. Q29 conducts during Storage Mode and allows the voltage stored on the individual capacitors to be applied to the input to the A/D Amplifier.

MEASURE/STORE MULTIVIBRATOR

The one-shot multivibrator, composed of Q25 and Q26 has dual synchronizing inputs. The Measure Pulse (approximately 20 milliseconds) is coincident with the conduction of Q26. The multivibrator is triggered at the end of each cycle by the trailing edge of the "4" time pulse. If C29 is sufficiently discharged, the trailing edge will cause the multivibrator to flop and Q26 to conduct, otherwise Q25 continues to conduct and the instrument remains in Storage Mode (approximately 320 milliseconds).

DISPLAY

The Display circuit is shown in Figure 10. Note that the +200 volts as shown in the timing diagram is high only during the last half of each digitizing time period.

The Decoder Driver accepts the BCD output from the Counter and translates it to a decimal ground, i.e., if the BCD count were "4-2" or 6, the Decoder Driver would place a ground potential on the "6" line to all of the display tubes. The anode of the appropriate tube would be allowed to receive the +200 volt pulse in the last half of the time period and display the 6. As an example, consider the "3" digitizing period which will place a HI on the base of Q69, causing it to conduct. Q69 conducting will lower the voltage on the base of Q73, which will cause it to conduct and allow the +200 volts to ionize V3 during the last half of the "3" digitizing period.

FACTS IN REVIEW:

a. Two Modes of operation, STORAGE and MEASURE.

b. Input is sampled only during MEASURE MODE and "1" digitizing time.

c. Sample and Hold is used only during MEASURE MODE.

d. ANALOG STORAGE receives its initial voltages during MEASURE MODE, but they are not used until the instrument is in STORAGE MODE.

8100A DIGITAL MULTIMETER OPERATIONAL THEORY

The 8100A consists of three main sections, referring to Figure 1 and the Schematic Drawings.

1. The Buffer section acts as a signal conditioner, capable of dividing voltage inputs, filtering and impedance conversion. The input divider also functions as a portion of the current source in the resistance ranges. (See Figure 2)

2. The Analog/Digital Conversion system, accepts the output from the Buffer and digitizes it using FLUKE'S Recirculating Remainder system of conversion. The unit samples three times a minute and recycles every 20 milliseconds.

3. The display section accepts the BCD output of the Analog to Digital Converter and puts it into ten line decimal output and displays the result on NIXIE tubes on a timed pulse basis.

In addition to the three main sections described above, the Power Supply serves dual functions. (See Figure 3 and Schematic No. 4). In addition to supplying the voltages required by the instrument it also contains an inverter that is used to both produce operating voltages for the instrument and supply the clock or synchronization for timing the instrument.

Power for the 8100A is supplied by either the AC power line or via the internal battery pack, as furnished with the −01 option. When operated from line voltage transformer,T101 provides two outputs. One output is rectified and filtered and used for the −18 volt supply in the instrument. The other winding provides a higher voltage which is rectified and used to charge the battery option, through DS11 which acts as a series limiting element.

The voltage supplied by the line voltage conversion is always greater than the voltage from the batteries, back biasing CR34 which prevents draining the batteries. The negative voltage, from either the batteries or the rectifiers CR1 and CR2, is regulated and filtered after passing through the protective fuse, F2, and then on to supply the instrument all of it's negative voltage needs.

The −18 volts operates a 250 Hz inverter consisting of Q4, Q5 and a driver transformer T102. The output voltages from T102 are then conditioned to supply the remaining potential needs of the 8100A.

A high voltage winding (100V) operates a doubler rectifier circuit which provides 200V dc. This +200V dc is used to pulse the readout tubes.

T102 also provides one output which is rectified and filtered to +5 volts which is used to supply all of the integrated circuit logic. Another winding of T102 provides a voltage which is rectified and regulated to provide the +15 volts needed as a positive supply in the instrument. This +15 volts is further dropped by a zener regulated circuit to provide the +7.0 volt reference needed in the 8100A. This +7.0 volt reference supply has a fixed load of 2 ma in R181 and is protected from current reversals when an overload occurs in the ohms configuration by CR10.

INPUT RANGE DIVIDER (Figure 2 and Schematic No. 1)

The function switching on the front panel will provide one of the four basic configurations shown in Figure 2. When the instrument is operated in the DC volts position the divider will provide divisions of 1, 10, 100 and 1000 in order to maintain a 1 volt input into the Buffer. The input divider consists of R156, R158, R159, R160 and R157 is provided for calibration.

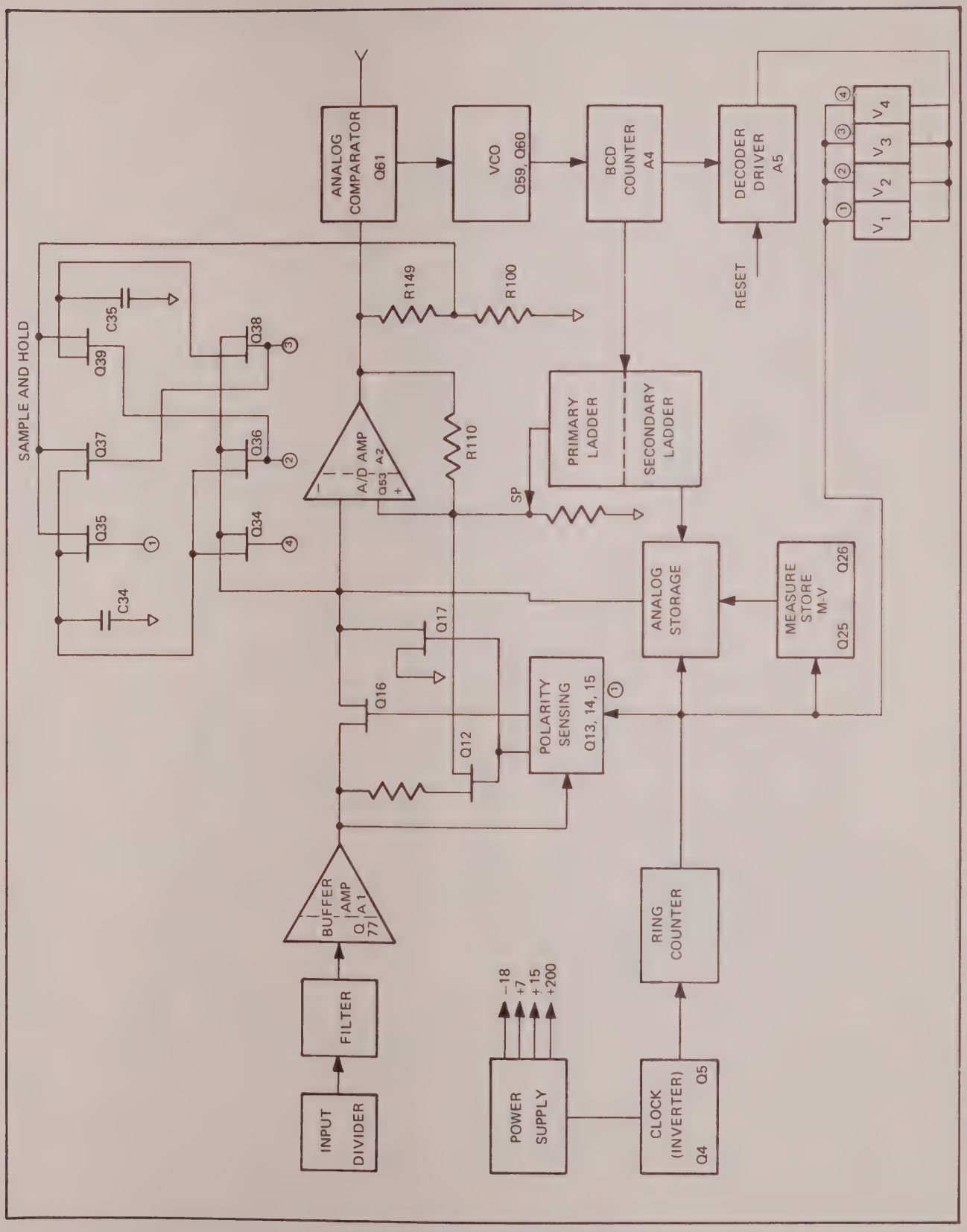


Figure 1. 8100 BLOCK DIAGRAM

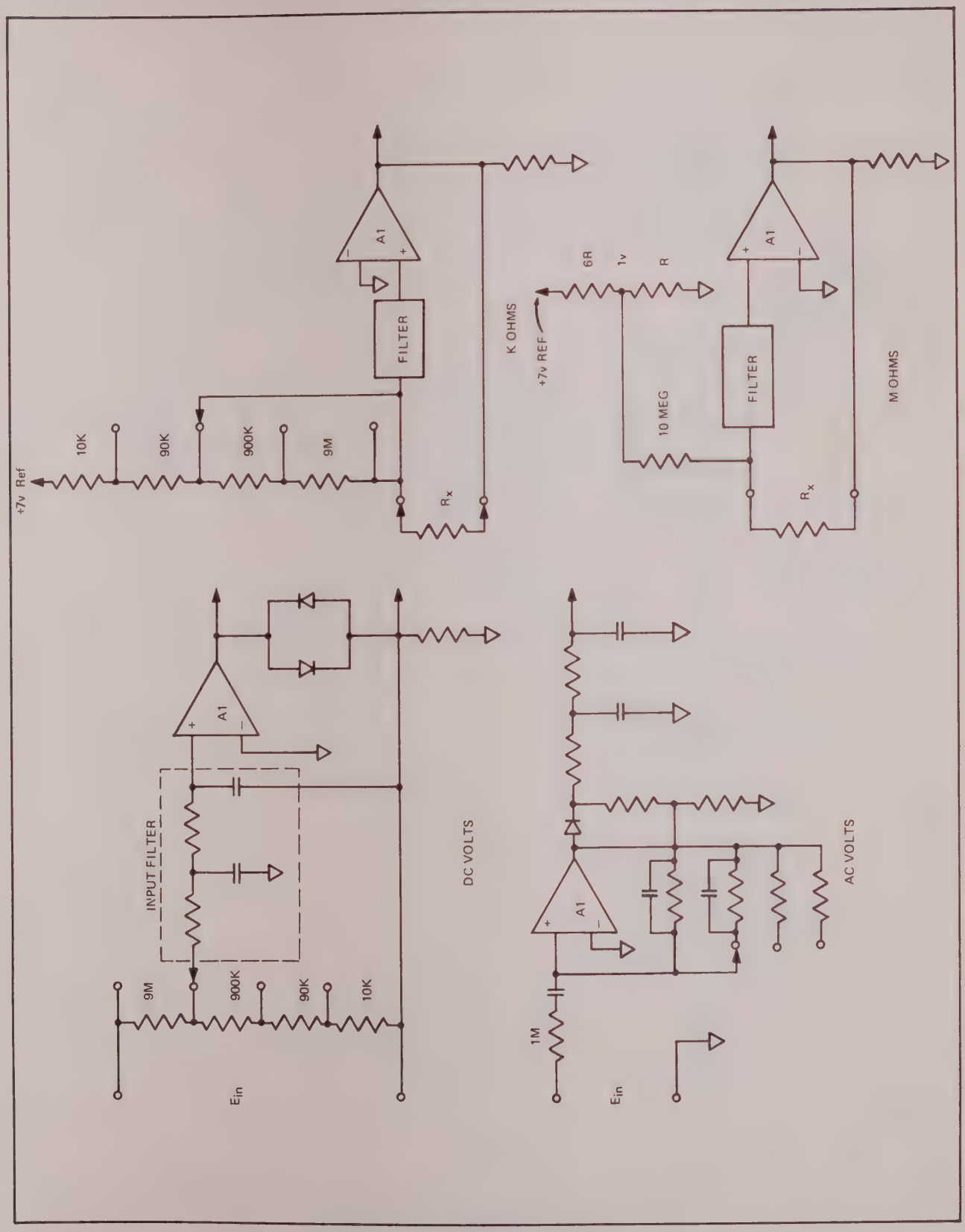

A1
FILTER
10K
90K
900K
9M
+7v Ref
Rx
K OHMS
6R
1v
R
+7v REF
10 MEG
M OHMS
INPUT FILTER
DC VOLTS
AC VOLTS
1M
Ein

Figure 2.

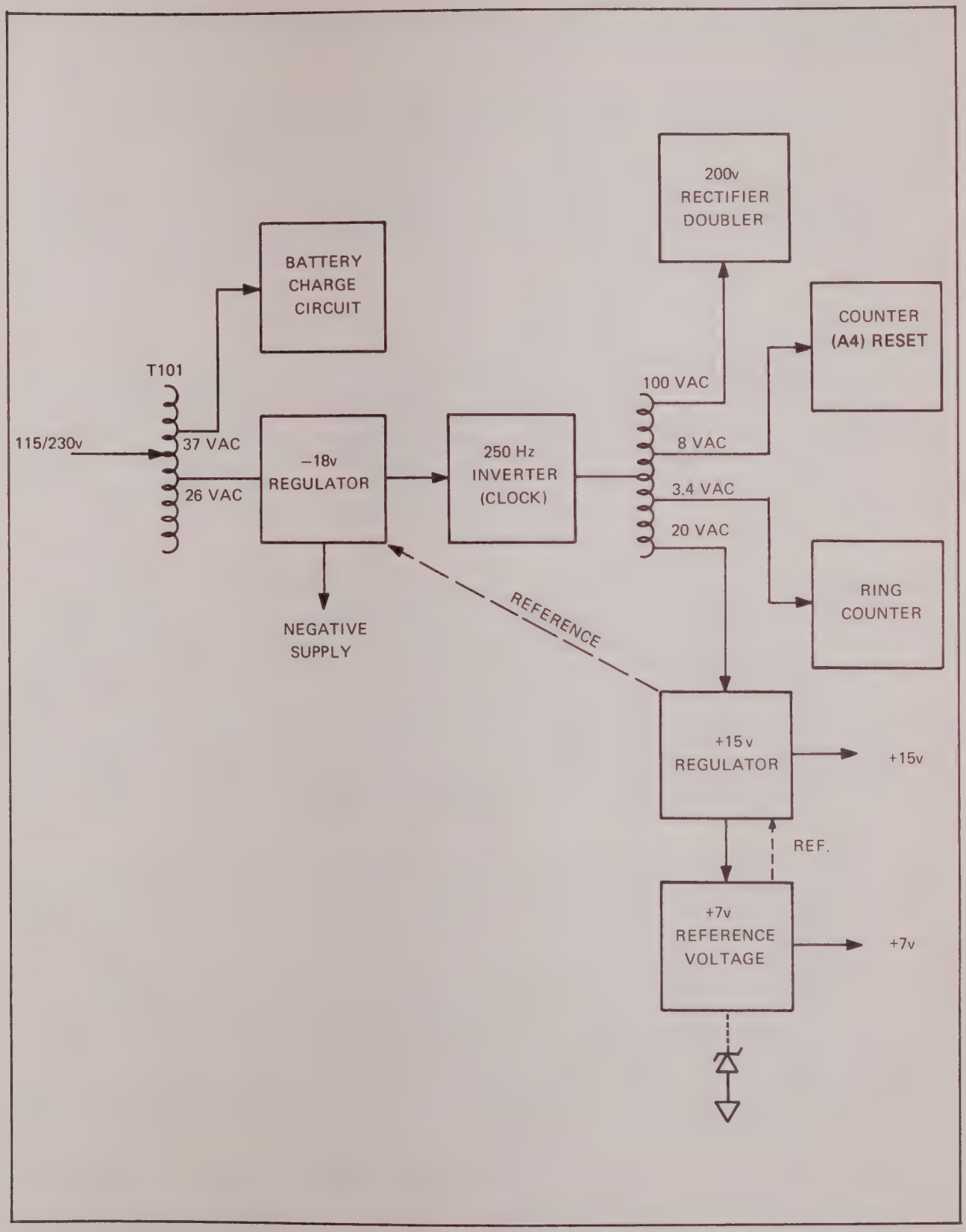


Figure 3. 8100 POWER SUPPLY

In the K Ohms function, the bottom of the input divider (R160) is removed from the common binding post and connected to the +7.0 volt reference supply. The divider now acts as the current supply for resistance measurements.

In the 10M Ohm function the bottom end of the range divider is connected to divider R152 and R154 which can be adjusted by R153 to provide 10M Ohm calibration.

When the AC Volts function is selected the input configuration is changed to an operational rectifier. A pair of rectifier diodes is placed inside a strong feedback loop. A negative feedback signal proportional to the input voltage is developed across R161, R162, R174 and calibration pot R34, which is fed to the A-D Amplifier.

INPUT FILTER

The output of the Range Divider is fed into a two pole, passive filter consisting of R27, R28, C10, C11, C12 and C13. (Filter switch out). The settling time is .25 sec and 60 Hz is attenuated about 20 db. With the Filter switch depressed, C10 and C13 are removed from the circuit and the settling time becomes 1 second and 60 Hz is now attenuated about 60 db. CR11 and CR12, together with R27 provide protection for both the filter and the Buffer amplifier from excessive voltage inputs. In the 10 volt range, R27 is switched out since the output impedance of the range divider is 1M Ohm and R27 is not needed.

BUFFER AMPLIFIER

Q77 is a low noise, low drive J-FET pair, operating in a common source configuration and serves as the input stage to the Buffer Amplifier configuration. R175 is the zero adjustment pot, which in conjunction with R176, R177 and R188 forms a network by which the initial offset of Q77 can be reduced to zero. The output of Q77 drives A1, a monolithic operational amplifier, which provides the bulk of the gain. C51 is placed around A1 to provide a smooth roll off through unity gain. Q79 is a common base output stage whose purpose is to raise the output impedance of the amplifier as high as possible. In order to avoid degrading the high output impedance, Q79 operates into a constant load current, Q80. The Buffer amplifier feedback loop is completed through diodes CR14 and CR15, which provide a voltage step around zero to drive the following polarity sensing circuit. R174 provides the load resistance for the amplifier.

When AC Volts function is selected, the buffer amplifier is connected as an operational rectifier with R24 as the input resistor, AC coupled through C9 and R29, R30, and R32 as the negative feedback ranging resistors. Diodes CR14 and CR15 now act as an operational rectifier. The positive half cycles only flow through CR15 and R162 where they develop a half wave rectified DC voltage proportional to the average value of the AC input. The high output impedance of Q79 and Q80 aids appreciably in improving the linearity at low levels where the threshold voltages of CR14 and CR15 tend to lower the amplifier loop gain. The half wave rectifier output is smoothed by two stage RC filter R35, C19, R36 and C20 to provide a 1 volt full-scale output for the A-D Converter. Because the input capacity of Q77, along with additional stray capacities, causes an additional pole in the loop response of the AC converter. Trimmer capacitors C14 and C15 are provided on the two lowest ranges to adjust the frequency response up through 20 kHz. The low resistances of R31 and R32 make this unnecessary on the two upper ranges.

A-D CONVERTER (Figure 1 and Schematic No's. 2 and 3)

The Recirculating Remainder conversion process is synchronously operated. That is to say; it progresses through it's steps in time with an internal clock, which is the Power Supply Inverter (250 Hz).

A Ring Counter fed by one of the outputs of T102, divides each cycle into five time periods of 4 milliseconds each as shown in Figure 4. The first time period is the ZERO time, this is the time period when the offset is removed from the A-D Converter amplifier. During the remaining four time periods each of the four digits is digitized and then displayed. At the end of the last period, the Ring Counter supplies a synchronizing pulse through R68 and C27 to the Measure Store Multivibrator Q25. It is the job of the Measure Store circuit to determine whether the A-D Converter will sample (Measurement Mode) the input voltage or continue to display the information held in storage (Storage Mode). See Figure 5 for sequence of operation.

POLARITY SENSING

Q13 turns on only when a 1 period time pulse appears at its gate and in Measurement Mode. This activates the Polarity Sensing Circuit. If the voltage at R40 is positive (Negative instrument input) Q15 will conduct and the signal from the Measure Store Multivibrator (Q25) will cause FET switch Q16 to conduct placing input on the A-D Amplifier.

If the voltage sensed by R40 is negative (Positive input to the 8100) Q14 will conduct and the signal at the collector of Q14 and the pulse from the Measure Store Multivibrator Q25 will turn FET switches Q12 and Q17 on. The negative output of the Buffer will be applied through the scaling resistors R50 and R51 and switch Q12 to the positive input of the A-D Amplifier. The Polarity Detector operates only while the instrument is in the Measurement Mode of operation and serves no function in the Storage Mode.

During time period 1, the amplified remainder is applied to C34. Q35 is prevented from conducting during the first half of the time period by the clock signal which is coupled through CR36 to its gate. During the second half of the period Q35 is ON and the amplified remainder is applied to C34.

During the second time period, Q35 is OFF and Q36 is ON which applies the remainder stored in C34 to be applied to the input of the Amplifier. Q39 is switched ON and the remainder is now applied to C35. Q39 is switched OFF during the third time period and Q37 and Q38 are switched ON which allows the remainder stored in C35 to be applied to the amplifier input.

During the third time period the remainder is stored in C34.

During the fourth and last time period Q34 is switched ON and the final remainder stored in C34 is applied to the input of the Amplifier.

ANALOG STORAGE

Clock pulses being applied through CR19 and Q28 allow conduction only during the second half of each time period. Q30 through Q33 are enabled only during the time period pulse corresponding to its gate connection.

During the last half of the 1 period the output of the Secondary Ladder is stored in capacitor C30. During the last half of the second period, the output of the Secondary Ladder is stored in C31. Etc.....

Q29 is enabled only when the instrument is in the Storage Mode and allows the output of each of the storage capacitors to appear at the input to the amplifier.

Analog storage is used only when the instrument is in the Storage Mode of operation as determined by the Measure Store Multivibrator.

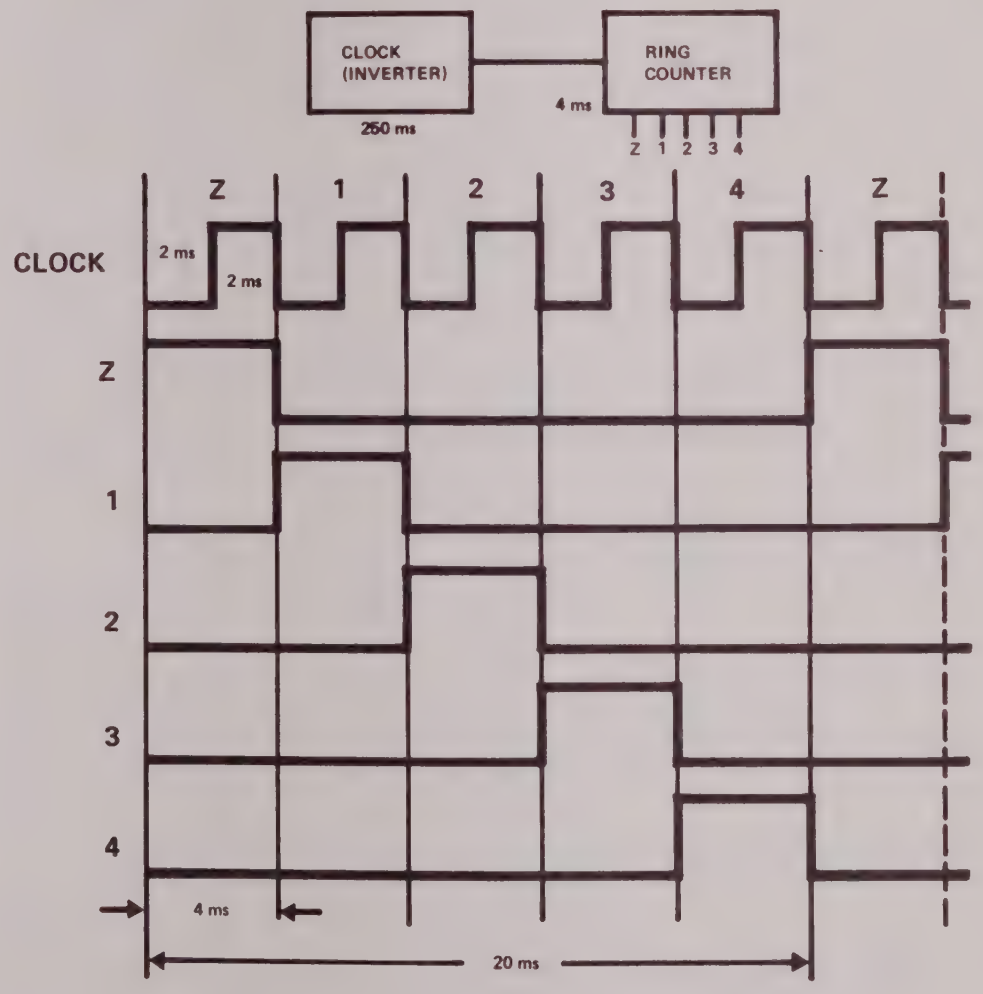
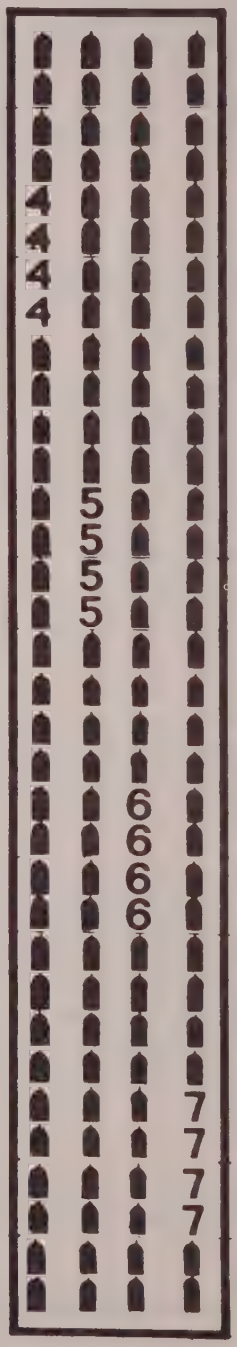


Figure 4. 8100 TIMING DIAGRAM

MEASURE MODE



Z — Internal error correction. (Offset removal)
1 — Sample input
1 — Sense and switch polarity
1 — Digitize first digit
1 — Display first digit
1 — Store remainder in Sample and Hold
1 — Store analog value in Analog Storage
1 — Disconnect input
1 — Display OUT
1 — Reset Counter
2 — Connect remainder from Sample and Hold to A/D Amplifier
2 — Digitize second digit
2 — Display second digit
2 — Store remainder in Sample and Hold
2 — Store analog value in Analog Storage
2 — Disconnect Sample and Hold from A/D Amp. input
2 — Display OUT
2 — Reset Counter
3 — Connect remainder from Sample and Hold to A/D Amp.
3 — Digitize third digit
3 — Display third digit
3 — Store remainder in Sample and Hold
3 — Store analog value in Analog Storage
3 — Disconnect Sample and Hold from A/D Amp. input
3 — Display OUT
3 — Reset Counter
4 — Connect remainder from Sample and Hold to A/D Amp
4 — Digitize fourth digit
4 — Display fourth digit
4 — If the fourth is the last digit, ignore any remainder
4 — Store analog value in Analog Storage
4 — Disconnect Sample and Hold from A/D Amp. input
4 — Display OUT
4 — Reset Counter

NOTE: Depending on the state of the Measure Store Multivibrator the instrument will return to "Z" time in either Measure Mode (unusual case) or enter Storage Mode.

Figure 5. 8100 DISPLAY SEQUENCE, MEASURE MODE

MEASURE STORE MULTIVIBRATOR

The one shot multivibrator formed by Q25 and Q26 has dual synchronizing inputs. The Measurement Cycle (approx. 20 ms) is coincident with the conduction of Q25. The Storage Cycle (approx. 330 ms) is coincident with the conduction of Q26. The multivibrator is triggered at the end of each complete cycle by the negative edge of the 4th time period pulse. If C29 is sufficiently discharged, this negative pulse will cause the multivibrator to pulse, sending a 20 ms measure pulse to the Polarity Sensing circuit which starts a measurement cycle. If the multivibrator does not pulse the 8100 remains in Storage Mode.

DISPLAY

It should be noted that each readout tube is on only during the last half of its corresponding time period. (2 ms on and 18 ms off).

The BCD output of the A4 Counter is fed to the Decoder Driver where it is translated into decimal output. If the BCD code was 3 the Decoder Driver will apply ground to the three line to all readout tubes. The 1 time period pulse, in conjunction with the clock pulse,which occurs only during the second half of each time period, will enable Q67 and Q71 thus allowing the +200 volts to light the three digit in V1.

EXAMPLE OPERATION (Figure 6) (Example voltage is .6532V)

Counter A4 is reset to zero as it is at the beginning of every time period by the pulse from A3A NAND gate.

The Ring Counter produces the ZERO pulse and Q18 and Q58 are turned on. Q58 connects C37, the zero holding capacitor, to the output of amplifier A2. Q18 connects the positive input of the amplifier to ground. This operation removes the offset for the remainder of the measurement cycle.

The Ring Counter produces the 1 time period pulse. It is necessary to assume that Q25 in the Measurement Store Multivibrator is conducting. The 1 pulse will turn transistor Q13 on. Since the .6532 volts into the instrument is positive, the voltage across R40 will be negative. Q14 will conduct which will cause Q12 and Q17 to turn on. These transistors were enabled by the Measure pulse from the Measure Store Multivibrator. The negative voltage from the Buffer will be applied to the A-D Amplifier through scaling resistors R50 and R51. Q17 connects the positive input to the amplifier to ground via resistors R186 and R187 which provide offset correction voltage to the positive input.

With R98, 200 kΩ, in the feedback loop and R51 and R50 as the input resistance the gain of the amplifier is 70. Q52 is used as temperature compensation only.

With .6532 volts at the input terminal of the amplifier, the output will attempt to go to 40 volts to satisfy the loop gain, but will be prevented from going so high by the limiting action of Q76 and R110. The output will exceed 7.0 volts and cause the Analog Comparator to conduct.

The Analog Comparator, Q89, will generate current at any time the voltage output of the Amplifier is seven or more volts. The current that it supplies is fed to the Voltage Controlled Oscillator.

MEASURE MODE	ZERO	1	2	3	4
Q18 & Q58 conduct and remove offset from A-D amp.	▬				
1 from Ring Counter enables Q13, polarity is determined and input FETs apply .6532 to A-D. 6 is digitized, remainder is stored in S & H C34. 6 is displayed and .6v stored in C30.		▬ ▬			
Input is disconnected from A-D amplifier.					
.532v from C34 is applied to A-D input. 5 is digitized and remainder .32 is stored in S & H C35. 5 is displayed and .5v is stored in C31.			▬ ▬		
.32 from C35 is applied to A-D amplifier. 3 is digitized and remainder .2 is stored in C34. 3 is displayed and .3v is stored in C32.				▬ ▬	
.2v from C34 is applied to A-D input and digitized. 2 is displayed and .2v is stored in C33.					▬ ▬
STORAGE MODE	**ZERO**	**1**	**2**	**3**	**4**
Q18 & Q58 conduct and remove offset from A-D amp.	▬				
Q30 conducts and applies .6v from C30 to A-D amp. 6 is digitized 6 is displayed and .6v is restored to C30.		▬ ▬			
Q31 conducts and applies .5v from C31 to A-D amp. 5 is digitized 5 is displayed and .5v is restored to C31.			▬ ▬		
Q32 conducts and applies .3v from C32 to A-D amp. 3 is digitized. 3 is displayed and .3v is restored to C32.				▬ ▬	
Q33 conducts and applies .2v from C33 to A-D amp. 2 is digitized. 2 is displayed and .2v is restored to C33.					▬ ▬
NOTE: If C29 is sufficiently discharged, the negative going portion of the 4 pulse will trigger the Measure Store Multivibrator and a measure pulse will be generated and a measure cycle will be started. If not another storage cycle will start.					

Figure 6.

The Voltage Controlled Oscillator, Q59 and Q60, will supply a series of pulses when supplied current. The repetition rate will be proportional to the current being supplied.

The pulses from the VCO are applied to the Counter A4, which is reset at the start of each time period. This counter translates the pulses into Binary Coded Decimal output. This BCD output is applied to the Ladder Switches and Drivers. As the BCD numerical value increases, the ladders produce 0.1 volt steps in their output. Thus in this case when the Primary Ladder output reaches .6 volts and is fed back to the input of the A-D Amplifier, the input difference to the amplifier becomes .0532 volts and the output of the amplifier will be less than 7 volts. When this occurs the Analog Comparitor Q89 does not furnish current to the VCO which causes it to stop pulsing.

The Decoder Driver translates this BCD output to decimal and produces a ground potential that is fed to all of the readout tubes 6 line. Only the 1 tube will light since it is the only one enabled by both clock and the 1 pulse via Q67 and Q71.

The Secondary Ladder feeds the Analog Storage circuit. Q28 is enabled only during the second half of each time period and Q30 is enabled by the 1 time period pulse. This causes C30 to be charged to .6 volts being furnished by the Secondary Ladder.

The remainder voltage during time period 1 was 0.532 volts at the input to the A-D Amplifier. This remainder is multiplied by the amplifier to 3.724 volts and appears across remainder resistors R99, R100 and R149. It is apparent that the total resistance is 14 Ω and that 2 kΩ represents 1/7 of the total resistance. This means that one seventh of the voltage appearing across the total remainder resistance appears across R100. This means, in the example case, .532 volts. This voltage will be applied across C34 in the Sample and Hold Circuit by the 1 time period pulse enabling transistor Q35. CR36 allows Q35 to be enabled only during the second half of the time period.

SUMMARY:

The highlights of the action that has taken place during the first time period are as follows:

1. The .6 volt was digitized.
2. .6 volt was placed in Analog Storage.
3. The remainder voltage .532 was placed in Sample and Hold.
4. The 6 was displayed during the last half of the time period by V1.

Time period 1 ends and transistor Q13 is no longer enabled as the 1 pulse is no longer furnished to it.

At the start of time period pulse 2 enables Q36 which applied the .532 volt remainder stored in C34 to appear at the input to the A-D Amplifier via Q18 which is enabled for the entire duration of The Measure Cycle. The .532 volts are amplified by 70 and once again the output of the amplifier exceeds the 7 volt reference causing Q89 to furnish current to the Voltage Controlled Oscillator. The pulse train produced is translated to BCD output and the Ladders are switched up in 0.1 volt increments until .5 volts is fed from the Primary Ladder to the summing junction of the A-D Amplifier. The input to the amplifier at this time is 0.32 volts which results in an output from the amplifier that is less than 7 volts and Q89 cuts off. The

BDC output from the A4 Counter is applied to the Decoder Driver and translated to decimal output, placing ground potential on all of the "5" lines to the readout tubes. The clock and 2 pulses enable Q68 and Q72 during the last half of the time period. Thus the readout tube V2 will display the "5" only during that last half of the time period.

The Secondary ladder will have an output of .5 volts at this time and it will be stored on capacitor C31 during the last half of the time period when Q28 conducts and Q31 is enabled by the 2 pulse.

The remainder, .032 volts will be amplified and divided by the remainder resistors and will be stored in the Sample and Hold circuit capacitor C35 via the enabled Q39 as .32 volts.

During period "3" Q38 will be enabled and apply the .32 volts, stored there, across the input to the A-D Amplifier through Q27.

The amplified voltage from the output of the amplifier will exceed the 7 volts of reference and Q89 will supply current to the Voltage Controlled Oscillator which will start a pulse chain. The pulses will be translated into BCD output. The BCD output will switch both Ladders and be decimalized by the Decoder Driver. When the output of the Primary Ladder reaches .3 volts the output of the amplifier will be less than 7 volts and Q89 will stop supplying current to the VCO. The decimalized "3" will appear as a ground potential on all of the 3 lines to the readout tubes. During the last half of the time period the +200 volts will be applied to V3 via Q69 and Q73 being enabled by the clock pulse and the 3 pulse thus allowing V3 to display the digit 3.

The .3 volts from the Secondary Ladder will be stored in Analog Storage capacitor C32 during the last half of the time period when Q28 is enabled and the 3 pulse has enabled Q32.

The remainder .02 at the input of the amplifier is amplified and appears across the remainder resistors and will be divided down to .2 volts and Q37 will be enabled causing this remainder to be stored in C34.

During time period 4 Q34 conducts applying the .2 volts stored in C34 to appear on the input to the A-D Amplifier. The output will exceed the reference voltage causing Q89 to supply current to the VCO which will start a pulse train. Counter A4 will count the pulses and translate them to BCD output. This BCD output causes the Ladder switches to operate and the output from the Primary Ladder is fed back to the summing point of the A-D Amplifier. When the output reaches .2 volts, the output of the amplifier is no longer higher than 7 volts and Q89 will stop conducting. The VCO stops pulsing and the Decoder Driver will translate the BCD output to decimal and apply ground potential to the 2 lines of all of the readout tubes. The clock and 4 pulses will enable Q70 and Q74, which will allow the +200 volts to light the tube V4 during the second half of the time period. The Secondary Ladder will have an output of .2 volts which will be stored in Analog Storage capacitor C33, the 4 pulse having enabled Q33 and the second half time period pulse having enabled Q28.

This completes a Measurement Cycle. As the 4 time pulse goes negative returning to zero potential it will cause Q25 (Measure Pulse) to conduct, only if capacitor C29 is sufficiently discharged. In this case it would not be possible for the instrument to start another Measurement Cycle as C29 would be fully charged.

SUMMARY:

It will be noted that each increment of voltage has been stored in the Analog Storage capacitor as follows:

C30 .6 volts
C31 .5 volts
C33 .2 volts

None of these stored voltages were used in the Measurement Cycle. C29 was fully charged and Q26 is conducting, which occurs during the Storage Cycles of the instrument. Q27 will be off and Q29 will be enabled until the Measure Store Multivibrator is operated again. Q26 will conduct for approximately 330 ms or about 16 cycles of the instrument. At that time C29 will be sufficiently discharged to allow Q25 to conduct when it receives a negative going pulse from the 4th time period pulse. Q25 will then conduct for approximately 20 ms or one Measurement cycle.

STORAGE CYCLE (Figure 7)

The ZERO pulse will again cause the offset to be removed from the A-D Amplifier by placing C37 across the output of the amplifier and grounding the input, as the result of Q18 and Q58 conducting.

The 1 pulse will cause Q30 to enable and the voltage stored on C30 (0.6 volts) to be applied to the input of the A-D Amplifier through Q29, which has been enabled by the Measure Store Multivibrator.

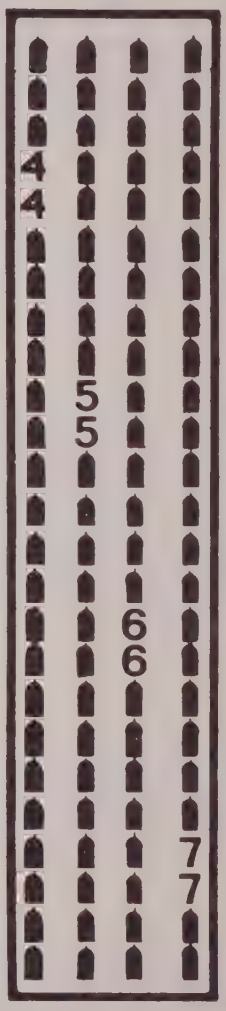
The A-D Amplifier amplifies the .6 volts by 70 and the output of the A-D Amplifier exceeds the 7 volt reference causing Q89 to conduct and supply current to the VCO. The VCO will start producing a pulse train. These pulses are counted and translated into BCD output by the action of Counter A4. The BCD output causes the Ladders to switch and increase their output by .1 volt per pulse. When the output of the Primary Ladder reaches .6 volts it will cause the A-D Amplifier to be satisfied and it will no longer have an output that is above the 7 volt reference of the instrument. The Secondary Ladder will have produced a .6 volt output which will be stored in C30 during the second half of the time period via Q28.

The Decoder Driver will have translated the BCD output to decimal and applied ground to all of the readout lamps on the 6 line. Q67 and Q71 are enabled, during the second half of the time period, by the clock and 1 pulses thus applying the +200 volts to V1 enabling it to display the 6.

During time period 2, Q31 and Q29 will conduct causing the .5 volts stored in C31 to appear across the input to the A-D Amplifier. The amplifier will have an output of more than 7 volts, which will cause Q89 to conduct and supply current to the VCO, which will produce a pulse train. The Counter A4 will count and translate the output to BCD. The Ladders will produce .1 volt of output for every pulse. The Primary Ladder being fed back to the input of the A-D Amplifier will cause the output of that amplifier to drop below 7 volts when .5 volts level is reached, which will cause Q89 to cut off and the VCO to stop producing pulses.

The Secondary Ladder will have produced .5 volts which will be stored on C31 during the second half of the time period by the conduction of Q28. The Decoder Driver will have placed ground

STORAGE MODE



Z — Internal error correction (Offset removal)
1 — Connect first analog value from Analog Storage to A/D Amp
1 — Digitize first digit
1 — Display first digit
1 — Restore first analog value in Analog Storage
1 — Display OUT
1 — Reset Counter
2 — Connect second analog value from Analog Storage to A/D Amp
2 — Digitize second digit
2 — Display second digit
2 — Restore second analog value in Analog Storage
2 — Display OUT
2 — Reset Counter
3 — Connect third analog value from Analog Storage to A/D Amp
3 — Digitize third digit
3 — Display third digit
3 — Restore third analog value in Analog Storage
3 — Display OUT
3 — Reset Counter
4 — Connect fourth analog value from Analog Storage to A/D Amp
4 — Digitize fourth digit
4 — Display fourth digit
4 — Restore fourth analog value in Analog Storage
4 — Display OUT
4 — Reset Counter

NOTE: Depending on the state of the Measure Store Multivibrator the instrument will return to "Z" time and in Measure Mode or recycle in Storage Mode.

Figure 7. 8100 DISPLAY SEQUENCE, STORAGE MODE

potential on the 5 lines to the readout tubes. Q68 and Q72 will be enabled by the 1 pulse and clock pulse during the second half of the time period. This applies the +200 volts to V2 causing it to display the digit 5.

During the 3 time period, Q32 will be enabled placing the .3 volts stored in C32 to be applied to the A-D Amplifier. The output of the amplifier will exceed the 7 volt reference and Q89 will supply current to the VCO which produces a pulse train. The pulses will be counted and translated to BCD output. This BCD output will cause the ladder switches to operate and cause the output of both ladders to increase by .1 volt for every pulse of the VCO. When the output of the Primary Ladder reaches .3 volts the A-D Amplifier will be satisfied and its output will drop below 7 volts causing Q89 to stop conducting, and the VCO will stop pulsing. The output of the Secondary Ladder (.3 volts) will be stored on C32 during the second half of the time period through Q28 which conducts only during the second half of each time period.

The Decoder Driver will have translated the BCD output to decimal and placed ground potential on all of the 3 lines to the readout tubes. Q69 and Q73 will have been enabled, during the second half of the time period, by the 3 time pulse and the clock pulse and the 3 will be displayed by V3.

Time pulse 4 will cause the .2 volts on C33 to be placed on the input to the A-D Amplifier whose output will exceed the 7 volt reference. Q89 will conduct and the VCO will pulse causing the ladder outputs to step .1 volt for every pulse received. When the output of the Primary Ladder, which is fed back to the summing point, reaches .2 volts, the output of the amplifier will no longer be higher than the 7 volt reference and Q89 will stop supplying current to the VCO. The Secondary Ladder will charge C33 to .2 volts and the action of the Decoder Driver will cause ground potential to appear on all of the 2 lines to the readout tubes. Q70 and Q74 will be enabled during the second half of the time period, at which time V4 will display the 2.

SUMMARY:

The capacitors in the Analog Storage Circuit will contain all of the increments of the voltage that were digitized during the previous Measurement Cycle. The Sample and Hold Circuit is disabled during all Storage Cycles. Each digit is displayed only during the last half of each time period. During the Storage Cycle the Polarity Sensing Circuit is not enabled.

This completes the Storage Cycle and as previously explained, the instrument will enter another Storage Cycle unless the charge on capacitor C29 has decreased to a value low enough to cause the Measure Store Multivibrator to pulse. If the Multivibrator does pulse a new Measurement Cycle will start and the input will be sampled again.

TROUBLESHOOTING: (Figure 8)

1. There are several ways of isolating the section of the 8100 that is malfunctioning. Observation of the readout and logical deduction based upon the knowledge of the theory of operation may be adequate to sectionalize the trouble.

2. The Power Supplies are interrelated and to isolate troubles in this area it may be necessary to isolate the −18 volt supply. To do this, disconnect the +15 volt end of R5 and connect it to an external source, or disconnect R35 and place a 1330Ω ±1% resistor from the base of Q3 to ground.

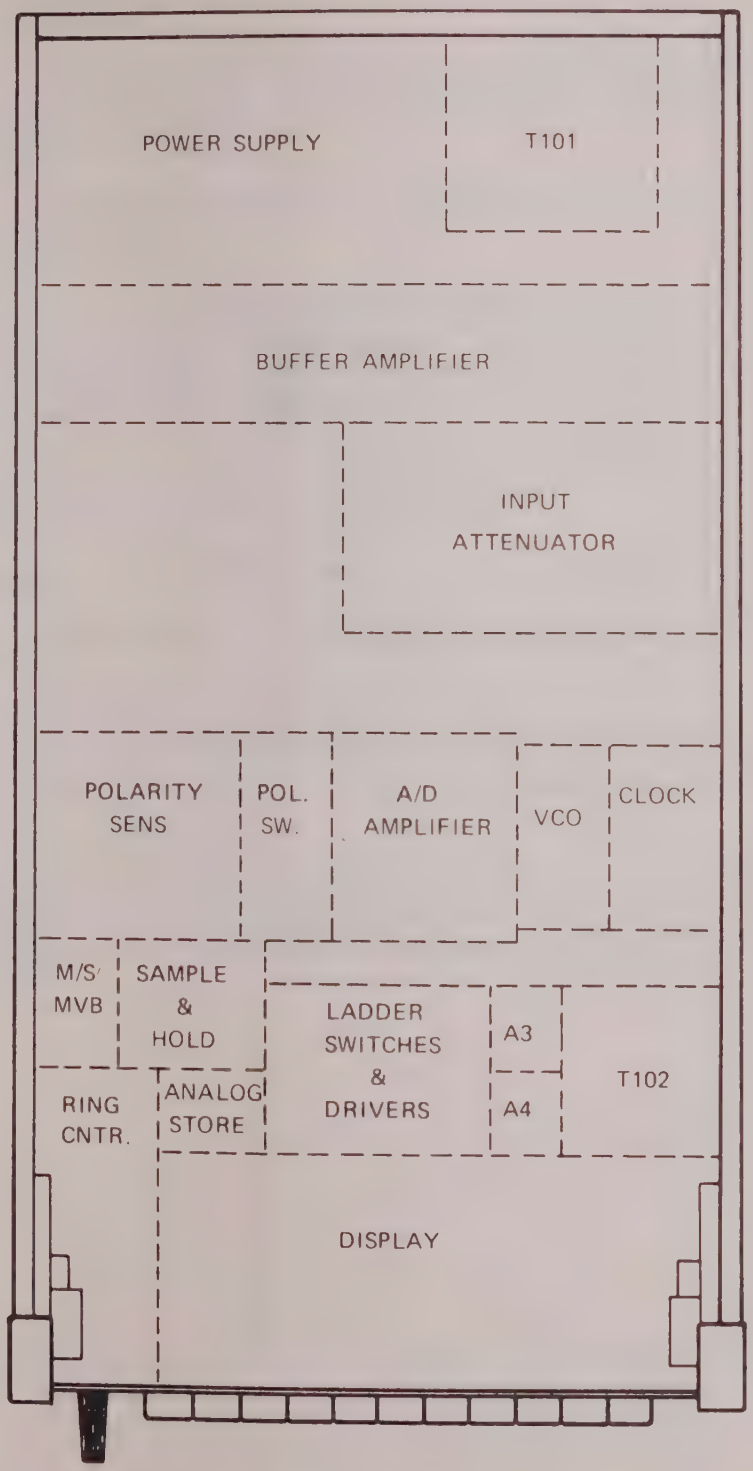


Figure 8. 8100 LAYOUT

3. The Input Buffer can be checked by measuring the voltage between TP9 and TP1 (ground), while measuring a voltage in the 1 Volt DC range. The voltage measured should be the same as the input but in reverse polarity.

4. The Auto Zero circuit will mask many types of trouble, so to disable this circuit it will be necessary to jumper TP6 to TP7 and jumper −18 volts to TP8. The measurement will now have an offset but the Auto Zero will be disabled.

5. Storage Mode can be avoided and the instrument placed in continuous Measurement Mode by placing a jumper between TP4 and TP5.

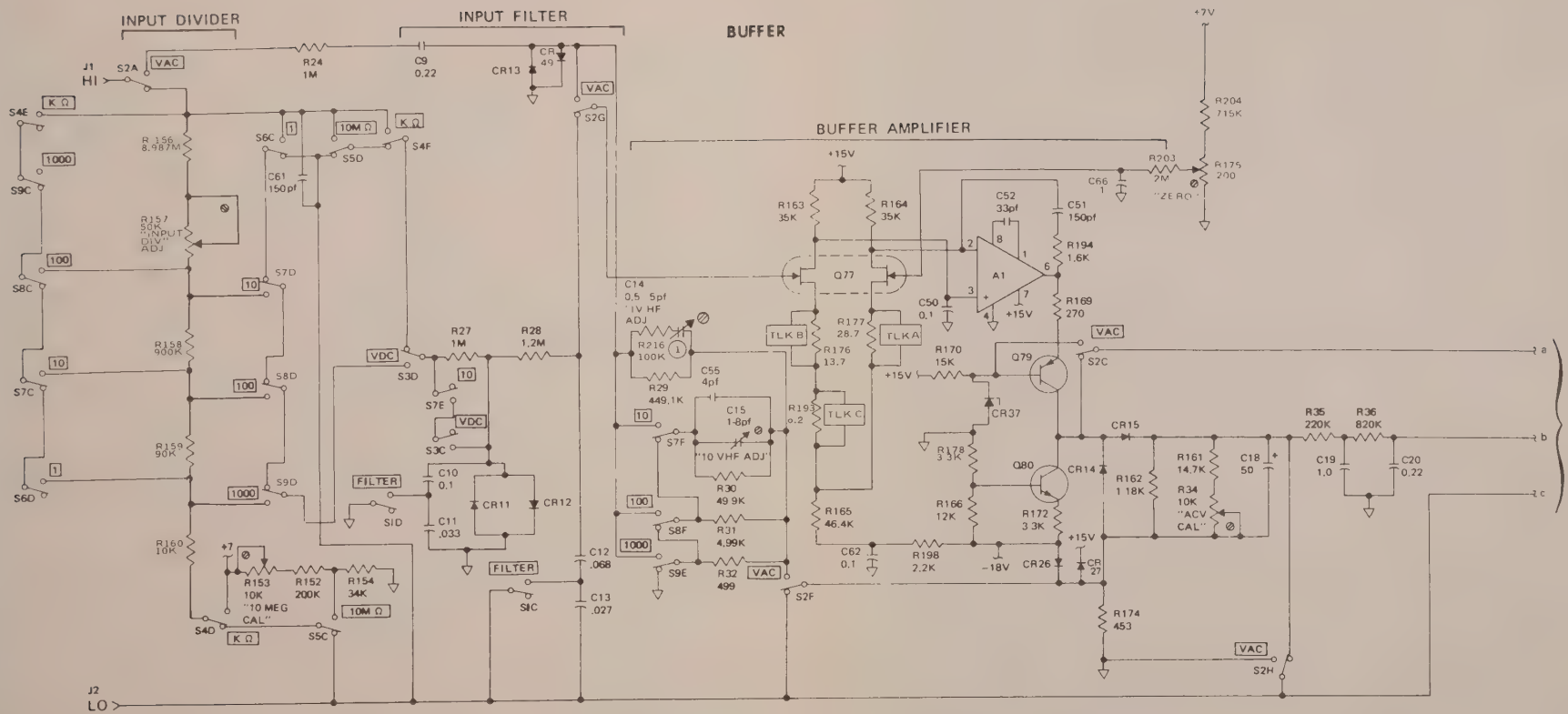
6. Connect +15 volt supply to the junction of R60 and R61, the Ring Counter will stop and the instrument will no longer display anything in the readout tubes. All of the output lines should measure −18 volts at this time. Remove the jumper and measure the collector voltage with an oscilloscope, each collector should measure about .3 volts when the transistor conducts.

7. An excessive load on any Ring Counter output can cause it to oscillate. Spikes following the time pulse indicate that the Ring Counter is near oscillation.

8. Trailing edge droop on the time pulses is caused by low gain transistors Q20 through Q28.

9. The following procedure will check the operation of the A-D Amplifier:

   a. Disable the Ring Counter by placing a jumper from +15 volts to TP11.
   b. Disable the Measure Store Multivibrator by placing a jumper from TP4 to TP5.
   c. Enable the Polarity Sense by placing a jumper from Q13 source to Q13 drain.
   d. Remove Binary Counter A4.
   e. Measure the voltage between TP2 and TP1 (ground).
   f. Apply 100 mv increments of input to the 8100. The measured voltage should increase 350 mv for every 100 mv increment of input and will be of the same polarity.



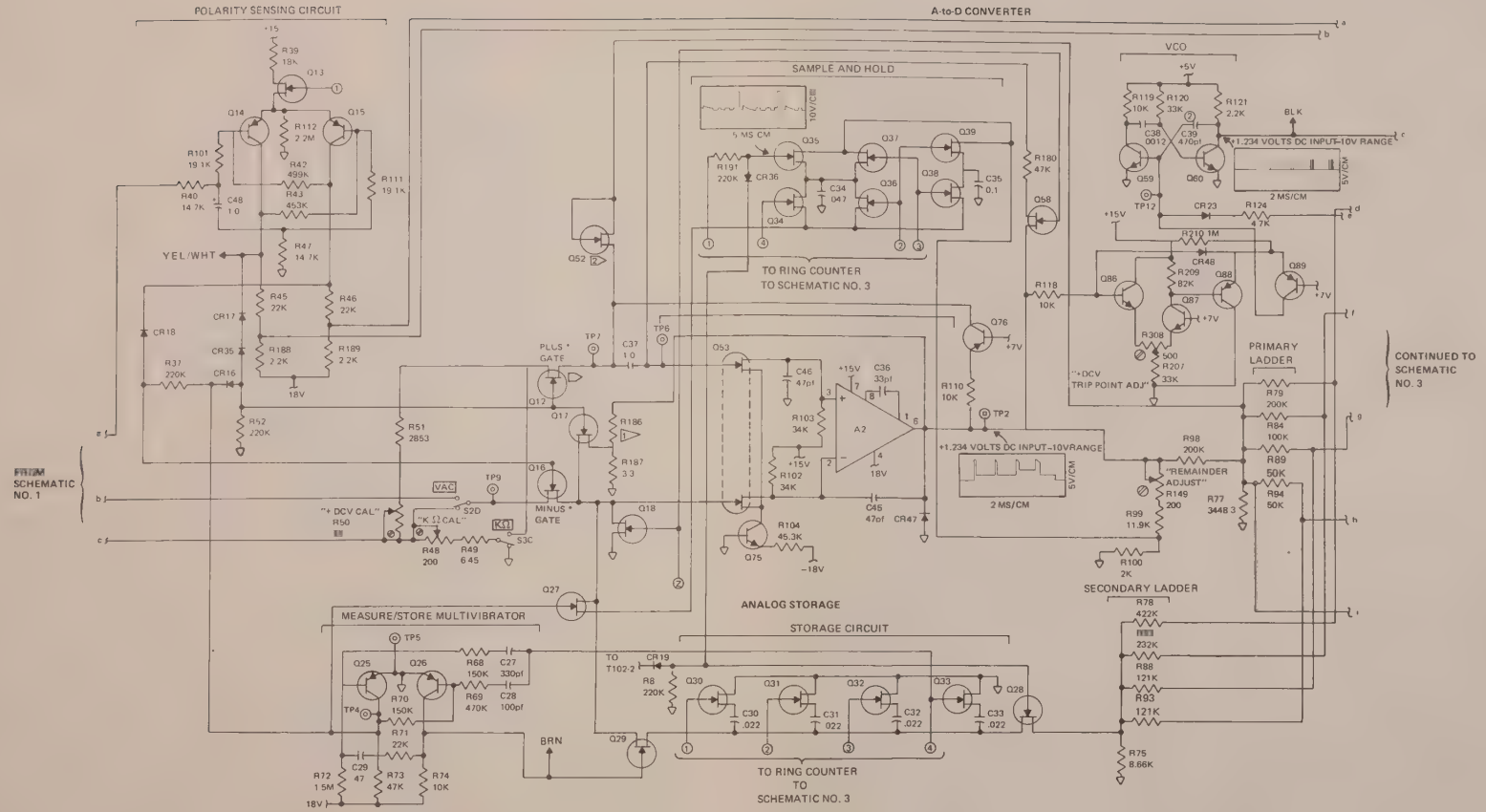
NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. ⟶ (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (–02).

CHANGES:

(1) R216 ADDED S/N 5050 AND ON

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER	
SCHEMATIC NO. 1	
SER. NO. 3410 THRU 3419 AND 4098 AND ON	REV C
JOHN FLUKE MFG CO., INC P O Box 7428 Seattle Washington 98133	



NOTES

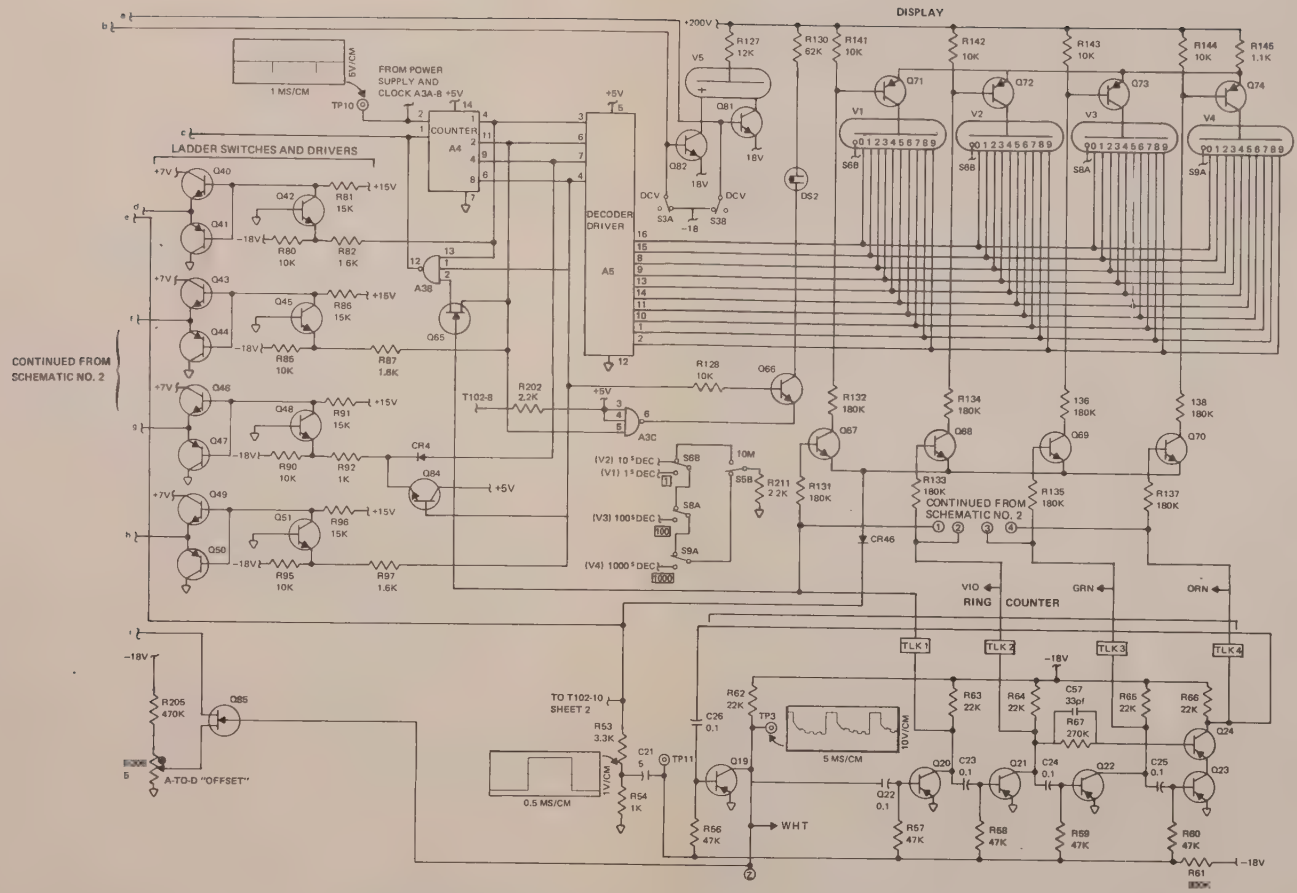
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. TLK TEST LINK.
6. 1 R186 SELECTED IN FINAL CALIBRATION.
7. (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (–02).
8. READOUT TUBE IN PIN LAYOUT:

	1°	°0	
	2°	°9	
	3°	°A	
	4°	°8	°LHD
RHD°	5°	°7	
	6°	°A	

BOTTOM VIEW

9. *PLUS GATE ON WITH POSITIVE INPUT, MINUS GATE ON WITH NEGATIVE INPUT.
10. 2 MATCHED FET PAIR.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A	
DIGITAL MULTIMETER	
SCHEMATIC NO. 2	
SER. NO. 3410 THRU 3419 AND 4098 AND ON	REV –
JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



NOTES:

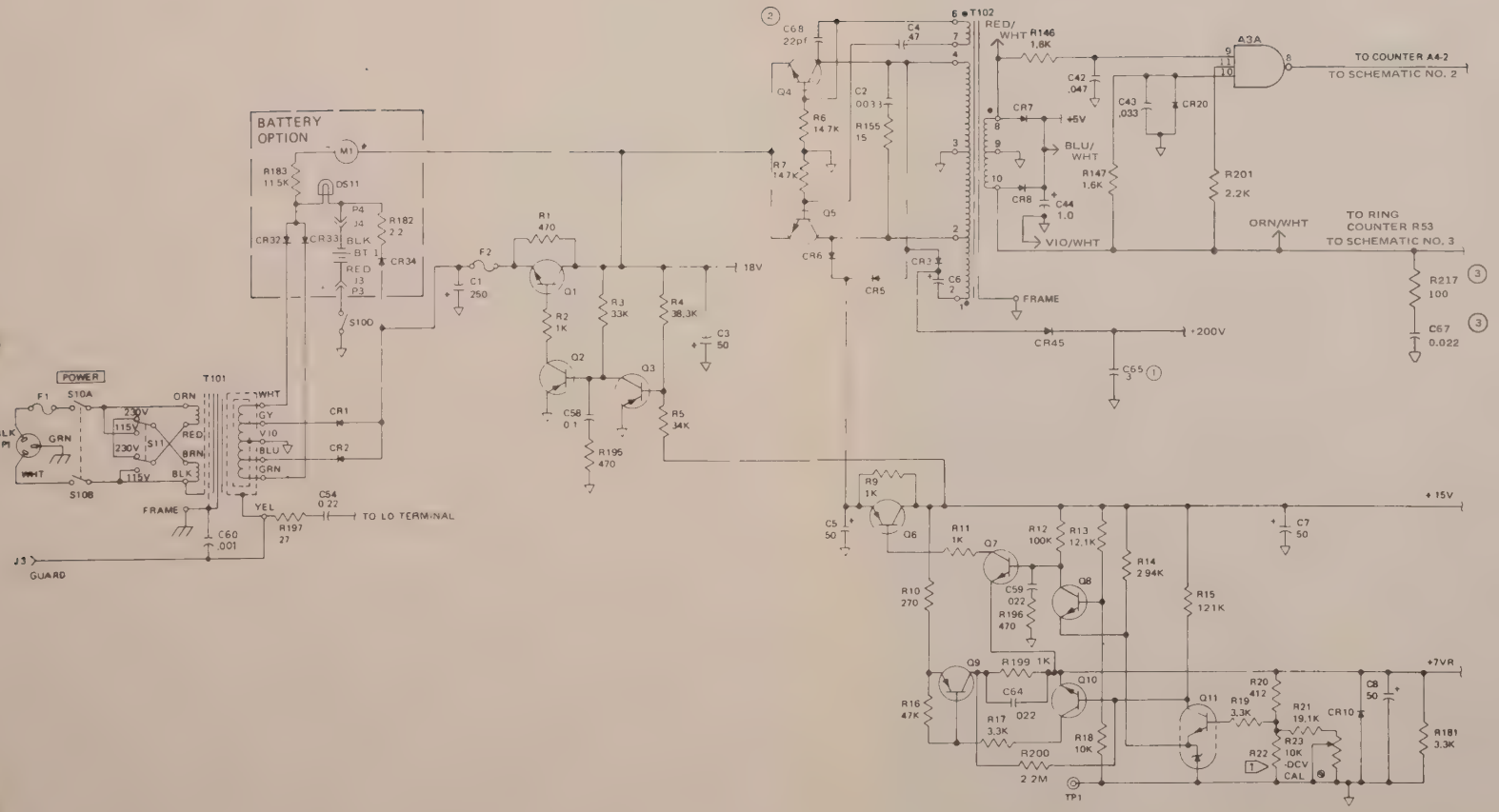
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL SWITCHES SHOWN IN OFF POSITION.
3. ⊘ DENOTES INTERNAL SCREWDRIVER ADJUSTMENT.
4. ▭ DENOTES FRONT PANEL LOCATION.
5. TLK TEST LINK
6. 1 R186 SELECTED IN FINAL CALIBRATION.
7. ⟶ (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (-02).
8. READOUT TUBE IN PIN LAYOUT:

	RHD°	°LHD
1°		°0
2°		°9
3°		°A
4°		°8
5°		°7
6°		°A

BOTTOM VIEW

9. "PLUS GATE ON WITH POSITIVE INPUT; MINUS GATE ON WITH NEGATIVE INPUT.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A	
DIGITAL MULTIMETER	
SCHEMATIC NO. 3	
SER. NO. 3410 THRU 3419 AND 4098 AND ON	REV –
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



NOTES :

1. [1] VALUE SELECTED AT TEST OF Q11

CHANGES:

(1) FOR S/N 3410 THRU 3419, 4098 THRU 4365, & 4429 THRU 4477: C65 WAS 4uf.

(2) C68 ADDED S/N 5050 AND ON.

(3) R217 AND C67 ADDED S/N 5018 AND ON.

(4) → (COLOR) CONNECTORS FOR ISOLATED PRINTER OUTPUT OPTION (–02).

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8100A DIGITAL MULTIMETER SCHEMATIC NO. 4	
SER. NO. 3410 THRU 3419 AND 4098 AND ON	REV -
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	

8200

The rapid and efficient repair of any instrument is greatly enhanced by a thorough understanding of the theory of operation. This course is designed to fill that need for experienced technicians who are engaged in the calibration and repair of the Fluke 8200A Digital Voltmeter.

The basic 8200A is a four-digit DC voltmeter providing 1, 10, 100, and 1000 volt ranges complete with automatic polarity, automatic ranging, and 60 percent over-ranging. It comes equipped to accept a variety of options. Each of the options can be installed in the field. The options available include the:

The –01 AC Converter Option provides four AC ranges with 30 Hz to 100 kHz response. Auto-ranging from the 1 VAC range to the 1000 VAC range is provided.

The –02 Millivolt DC Option provides two ranges of millivolt measurement; a 10 mV range and a 100 mV range. It provides automatic polarity, and the instrument will autorange down into the 100 or 10 mV range, from the VDC ranges. Autorange up from 10 or 100 mV range to VDC ranges is also provided.

The –03 Resistance Option provides six resistance ranges from 100 ohms to 10M ohms, and it is overload fused at 30V RMS. Autoranging has been included in the Resistance Option.

The –04 Isolated External Reference option; it is necessary that the instrument be provided with an –05 Option, which is the Rear Input option, when an Isolated External Reference Option is installed because of the limitation of the three front panel terminals. The Isolated External Reference will provide four terminal measurements: real-time ratio determinations, DC to DC in four ranges in the basic instrument, and AC and millivolt ratios when the options are installed.

The –05 rear input option provides a five-pin connector. Offering Signal HI and LOW, Guard, and External Reference HI and LOW.

The –06 Printer Output Option provides digits, polarity, and range information. Digits information and range information is given in Binary Coded Decimal format and in parallel output. The interface logic levels are +5V and 0V, and it can be used with the Remote Control Unit; –08 Option.

The –07 Data Output Option offers digits, polarity, and range in BCD format for digits and range in 8421 parallel or 4-bit serial format. The logic levels are +5V and 0V. It provides control input for an external trigger, automatic triggering, and time-outs enabled or disabled. It can be used with the 08 Remote Control Unit option. The Isolated Data Output option cannot be installed simultaneously with the 06 Isolated Printer Output option. The instrument can only accept one of the output options.

The –08 Remote Control Unit control, or program control, will interface with DTL or TTL. The Remote Control Unit requires +5V of DC at 105 mA from either the Data Output option or the Printer Output option. If the instrument is not equipped with either of these options, a special supply accessory is available, or it must be supplied from an external power supply. The Remote Control Unit option provides a remote flag, interlock protection, and address controlled by triggers.

In addition to the options provided for the 8200A, several accessories interface with the instrument. The A90 AC-DC Current Shunts, the 80F-5 High Voltage Probe, the 80F-15 High Voltage

Probe, the 80 RF Probes, and the rack-mounting hardware for either offset center or side-by-side installation.

MAIN BODY OF TEXT

BLOCK DIAGRAM

As can be seen in the block diagram (Figure 1), the instrument consists of several basic blocks; the Power Supply, Buffer, A-D Amplifier, Logic Control, Display, and the Inter-Connect assembly. Within the Power Supply four separate voltages are sourced: A +200V DC supply for the display tubes, a +15V DC, and a −15V DC operating supplies, and a +5V DC logic supply.

BUFFER (Figure 2)

The Buffer is an operational amplifier with a gain of one inverted. If the Buffer sees a +1V at its input terminals, it will produce a −1V at its output terminals. The primary purpose of the Buffer is isolation and impedance matching. The Buffer assembly also contains the Range Divider for DC giving division ratios of 1/1, 10/1, 100/1, and 1000/1. It contains a switchable four-pole active filter which provides losses in excess of 60 DB at 50 Hz cycles, greater than 65 DB at 60 cycles, and 100 DB or more at 200 cycles and above. The Buffer also contains its own Logic circuitry for range and function switches.

A-D ANALOG (Figure 3)

The A-D Analog assembly is made up of several circuits: the Polarity Detector and Switching circuit which provides the instrument with its automatic polarity detection and indication. It contains the Sample and Hold circuitry that is used when the instrument is initially digitizing a measurement. The +7V DC Reference Supply is also contained within the A-D Analog module, as is the Current Oscillator Modulator, the Ladders, and the Display Storage network.

LOGIC CONTROL (Figure 4)

The Logic Control contains the Constant Current Oscillator and the Counter. In addition, it also contains the Master Clock, which generates the basic timing for the instrument. The Master Clock feeds the Shift Register which generates the five timing periods; ZERO and the four digitizing periods. In addition, a Sample Oscillator is provided that feeds both the Shift Register and the Analog Control circuitry. The Sample Oscillator provides the Measure and Storage pulses. In addition, the Analog Control assembly provides gating pulses that are required for the special switching requirements in Recirculating Remainder. The Sample Oscillator also feeds the Shift Register to synchronize the start of Measurement time with the Master Clock and the Shift Register.

DISPLAY (Figure 5)

The Display assembly contains four circuit functions; Anode Strobing, Polarity Memory, Decoder Driver, and the Display. Anode Strobing, using the timing pulses from Logic Control, turns the display tubes ON in the proper sequence. The Polarity Memory circuit is a bi-stable multivibrator that receives information from the Polarity Sensing circuits in the Buffer, and holds that information in "memory" until it is displayed. The Decoder Driver is a sixteen state, monolithic device used to translate the Binary Coded Decimal information from the Counter, into decimal information to be used in order to ionize the proper digit in each display tube. The Display circuitry consists of the various interconnections required for supporting the illuminated display tubes and lights.

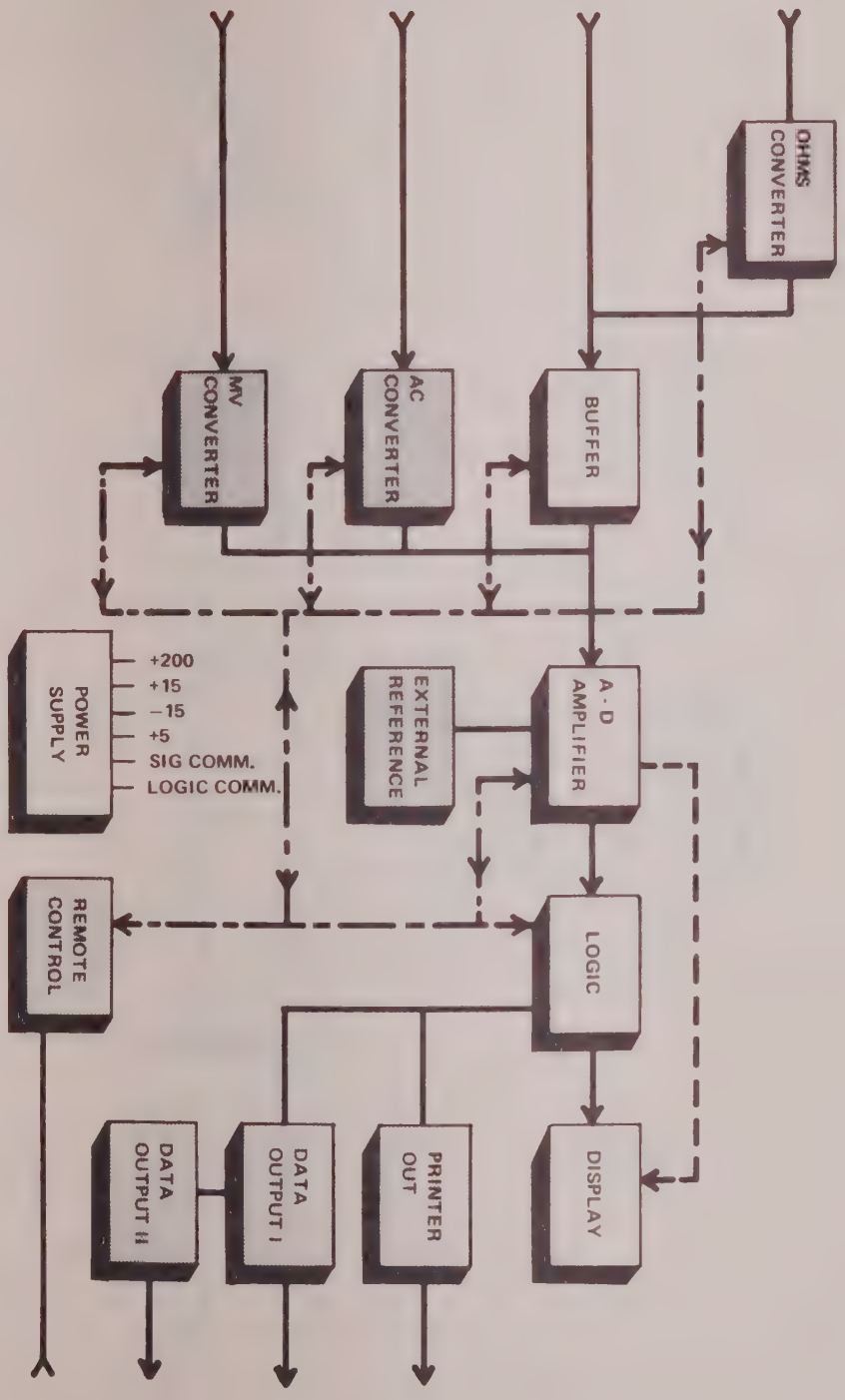


Figure 1. BASIC 8200A

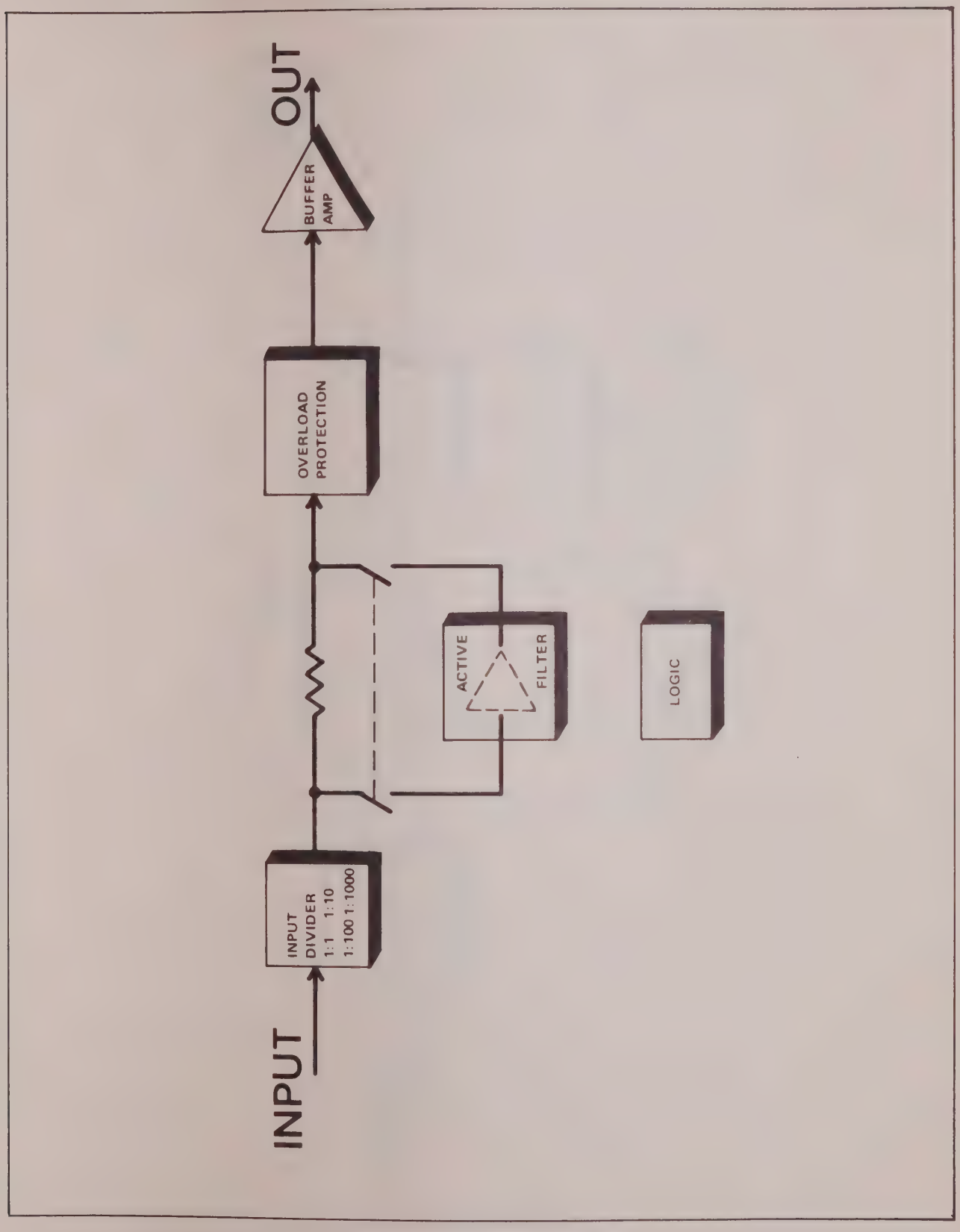


Figure 2. BUFFER (A4)

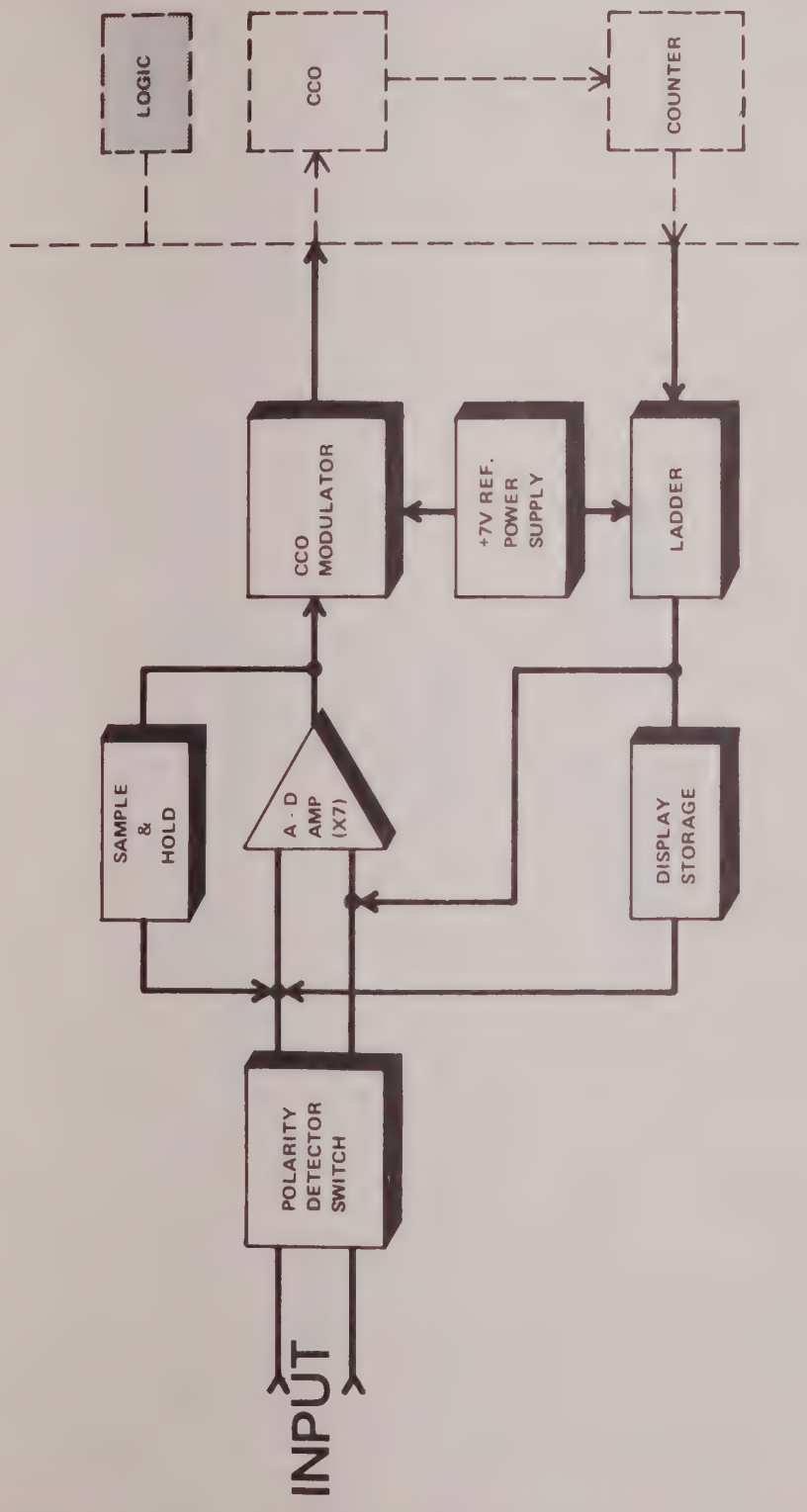


Figure 3. A TO D ANALOG (A7)

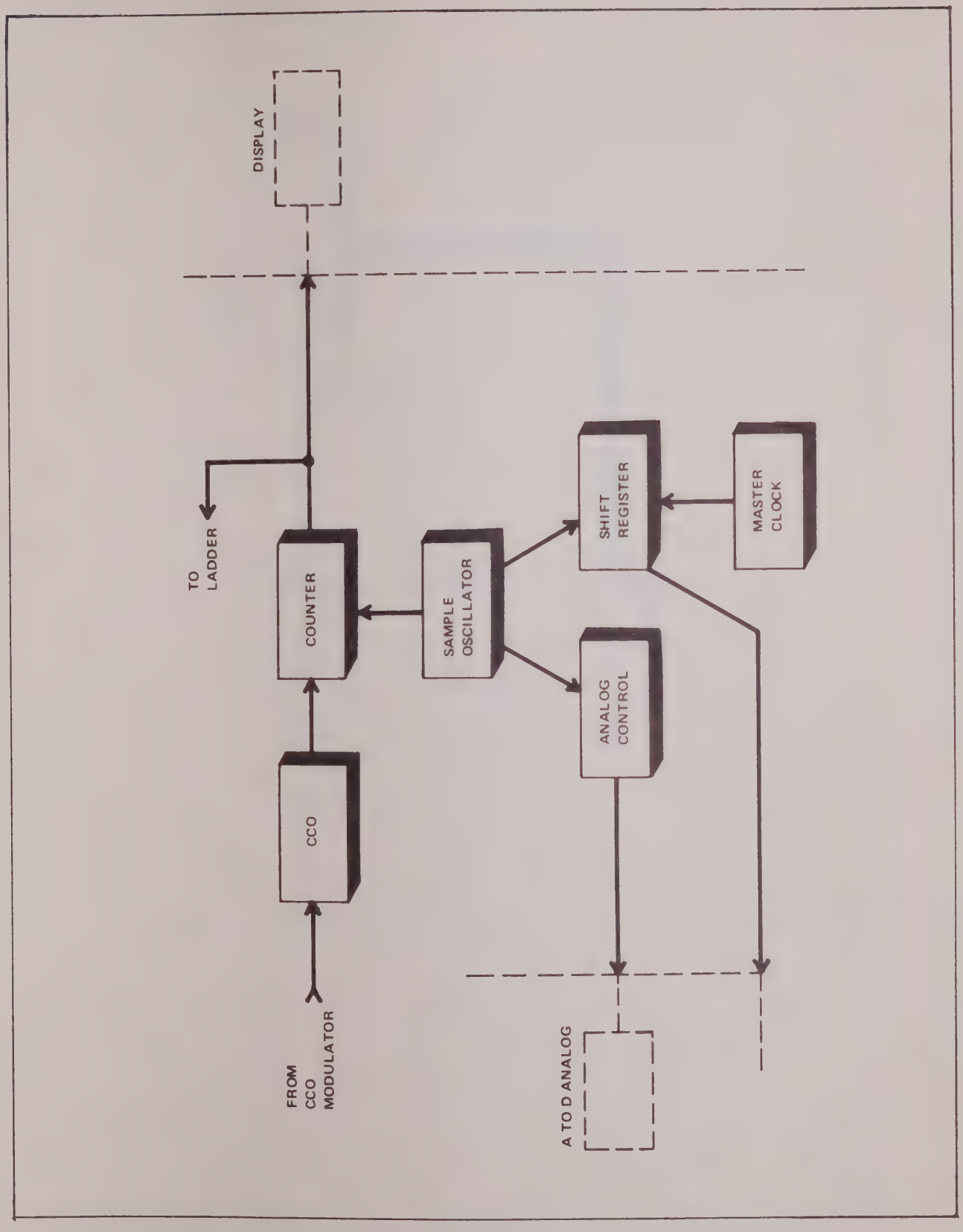


Figure 4. LOGIC CONTROL (A6)

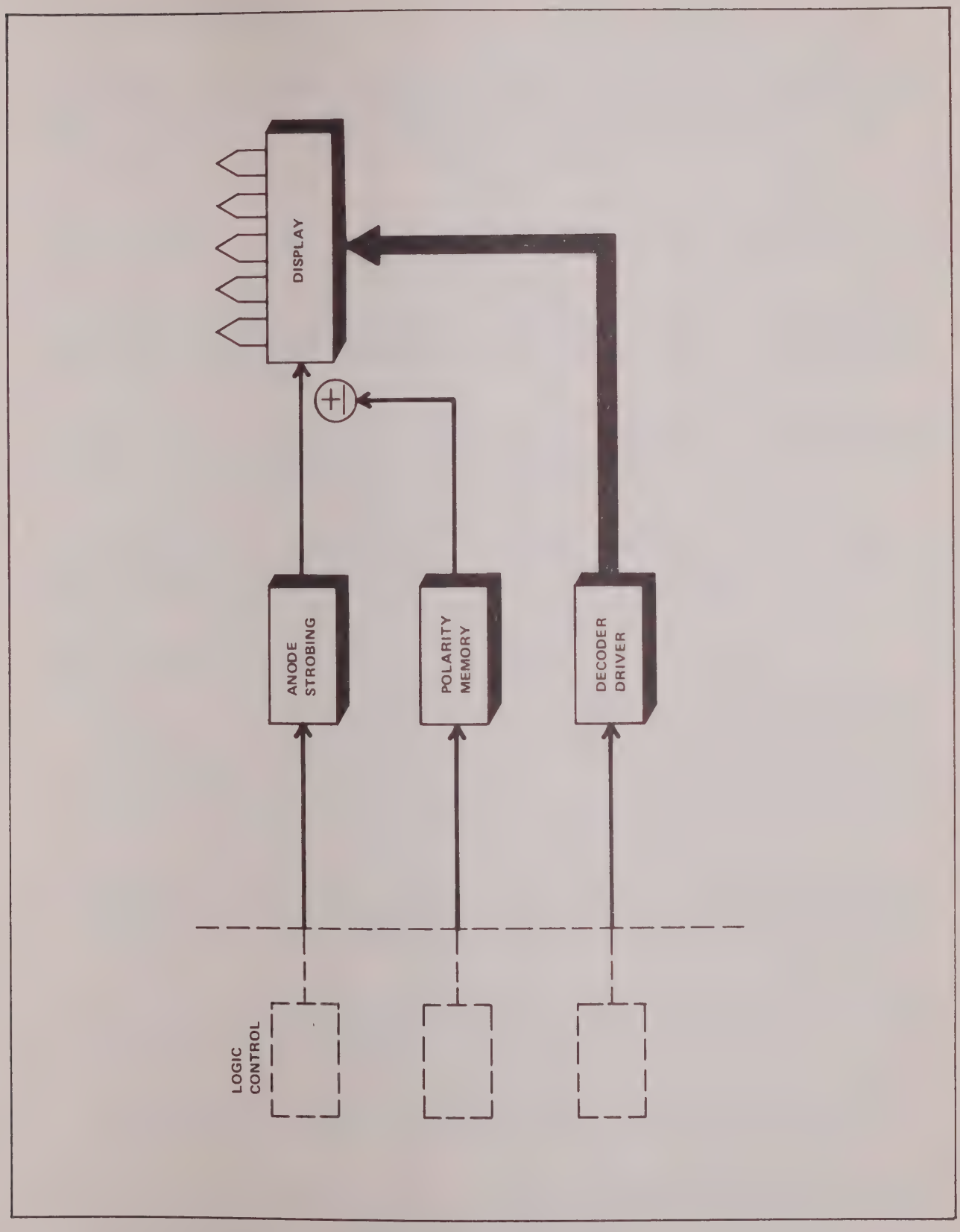


Figure 5. DISPLAY (A12)

INTERCONNECT (Figure 6)

The Interconnect assembly contains the circuits used for Range Command, Function Command, Range Register, and the Lamp Assembly used to display function selection. The Function and Range Command circuitry consists of the manual push-button switches used for selection. The Range Register contains the circuitry used in the autoranging functions.

OPTIONS (Figures 7, 8, and 9)

Figures 7, 8, and 9 are the block diagrams of the Option assemblies. Each of the options contains its own Logic circuitry, in addition to the circuitry to support its functional purpose.

The AC Converter, shown in Figure 7, contains two operational amplifiers; one used in the input to the rectifier, and one which is used to match the output impedance of the Filter to the input to the A/D circuitry. Range switching is accomplished by switching the resistors in the feedback loop of the AC operational amplifier.

The MV Converter, shown in Figure 8, contains a Filter and an operational amplifier with two feedback loops. These feedback loops control the gain of the amplifier. In the 10 mV range the amplifier has a gain of 100, and in the 100 mV range it has a gain of 10.

The Ohms option uses the +7 volt reference voltage, as shown in Figure 9, through series resistors to develop a voltage across the Rx or resistance to be measured. The resulting voltage across the unknown resistor is translated into an ohms measurement. This option feeds the Buffer assembly rather than feeding the A/D Analog assembly as do the other Options.

BLOCK DIAGRAM EXAMPLE VOLTAGE MEASUREMENT

Referring to the full block diagram given in Figure 10, the operation can be described as follows:

1. The input is applied to the buffer and divided down so that the output of the attenuator will be within the range of ZERO to 1.6 volts. The Filter is selected or not selected and the signal is passed to the Buffer Amplifier which has a gain of one and whose output is inverted. It is the purpose of the Buffer to keep the input impedance as high as possible while matching the impedance of the A-to-D Amplifier circuit which follows it.

2. A-to-D Analog Amplifier assembly receives the signal at the Polarity Detector which operates the FET switches applying the proper polarity to the A-to-D Amplifier which has a gain of 70. When the output of the amplifier is greater than the 7 volts, the CCO Modulator will produce current.

3. Current from the CCO Modulator is fed to the Logic Control assembly, where it is fed to the Current Control Oscillator. The Current Controlled Oscillator produces a pulse train. This pulse train is fed to the BCD Counter.

4. The BCD Counter counts the pulses from the CCO and feeds BCD information to the Decoder Driver which will furnish a ground to the proper numeral line to all of the display tubes.

5. The BCD Counter output is also fed to the Ladder Switches and Drivers and each BCD count causes the Ladder outputs to advance by 0.1 a volt. The output of the Primary Ladder is fed back to the input to the A-to-D Amplifier.

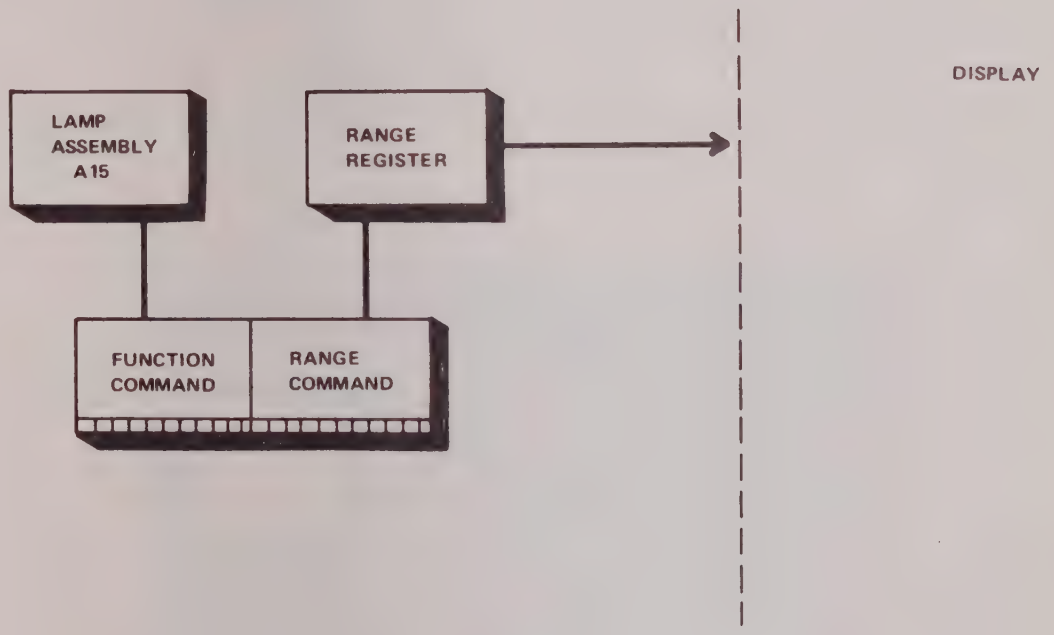


Figure 6. INTERCONNECT (A13)

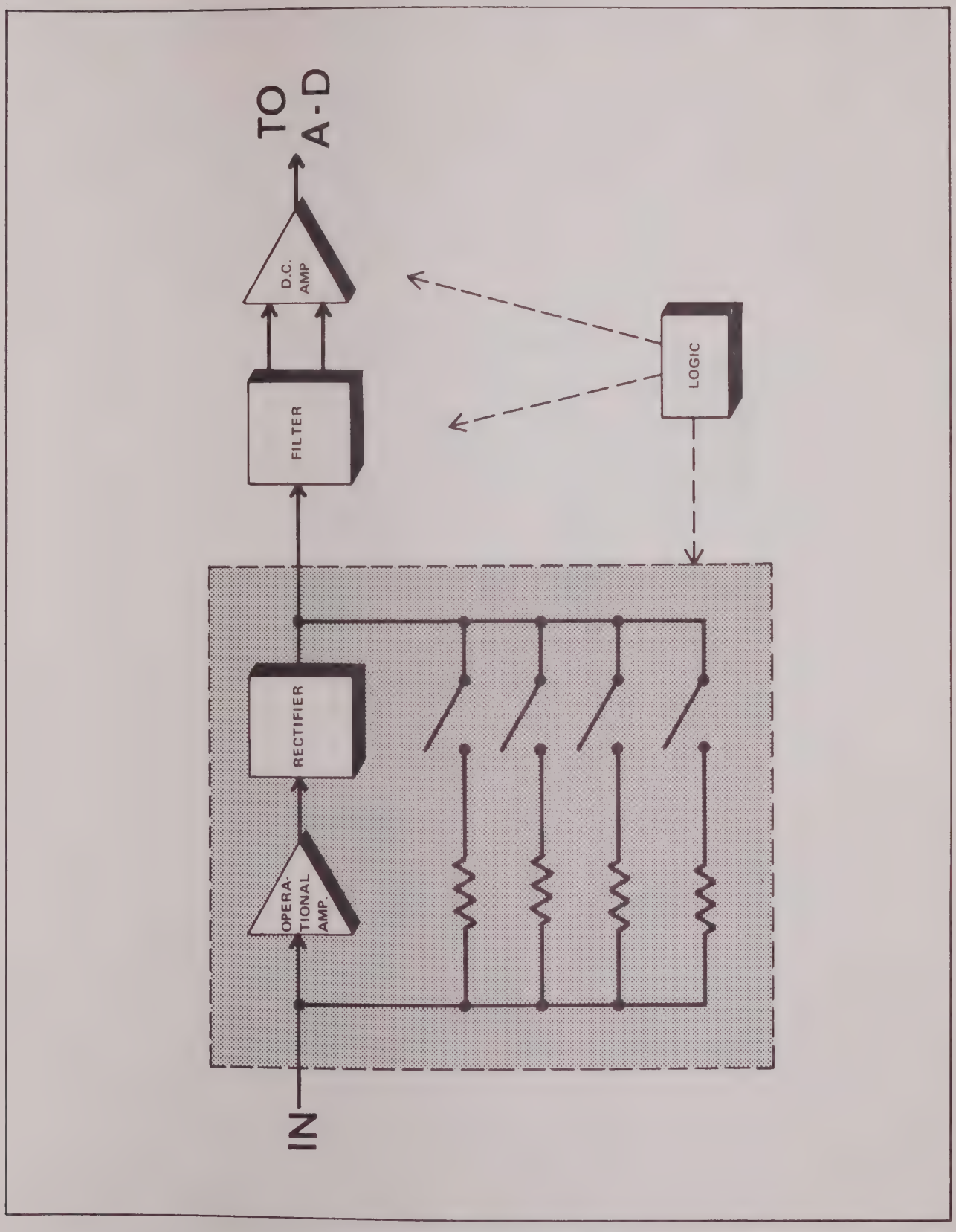


Figure 7. AC CONVERTER –01

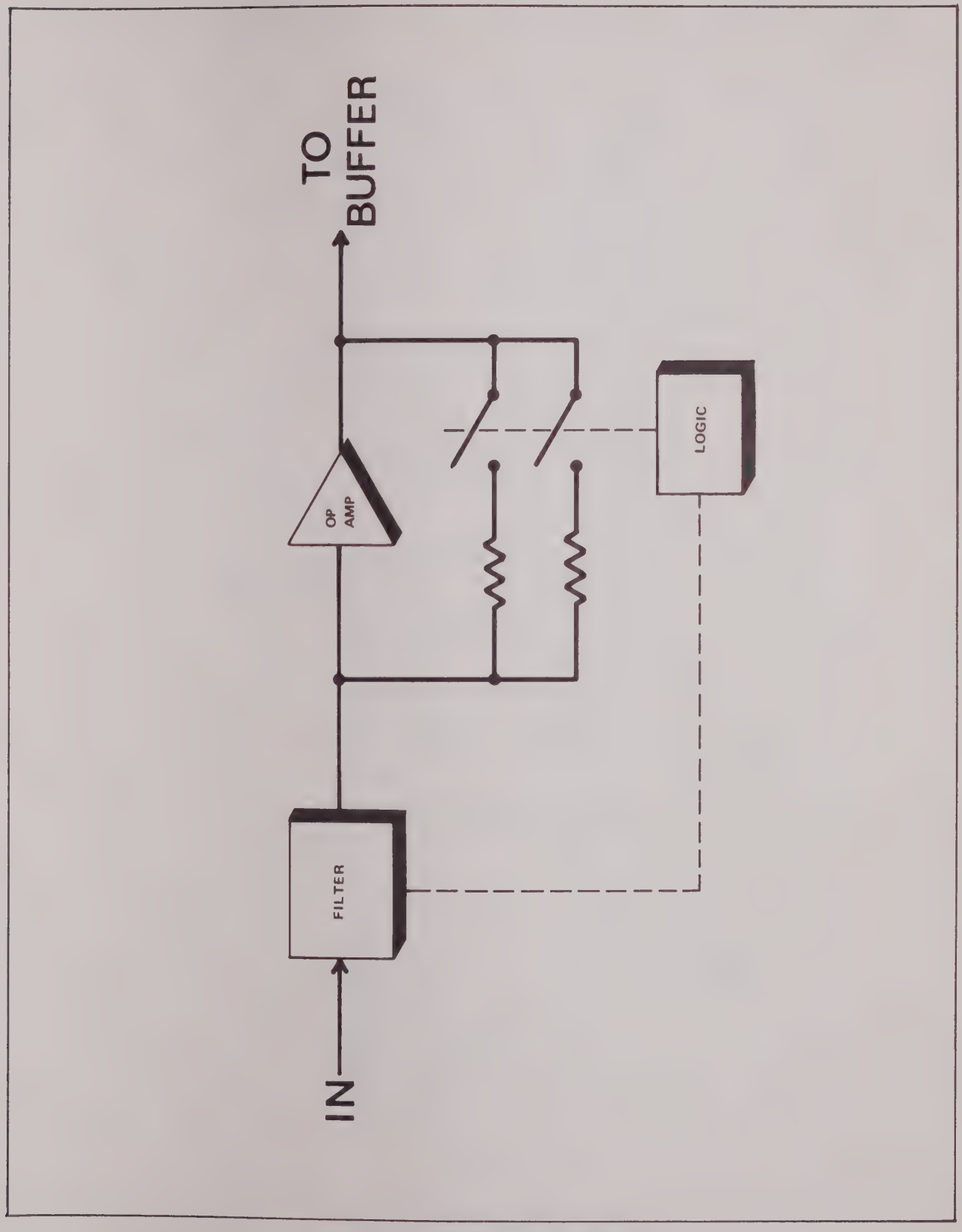


Figure 8. MV CONVERTER –02

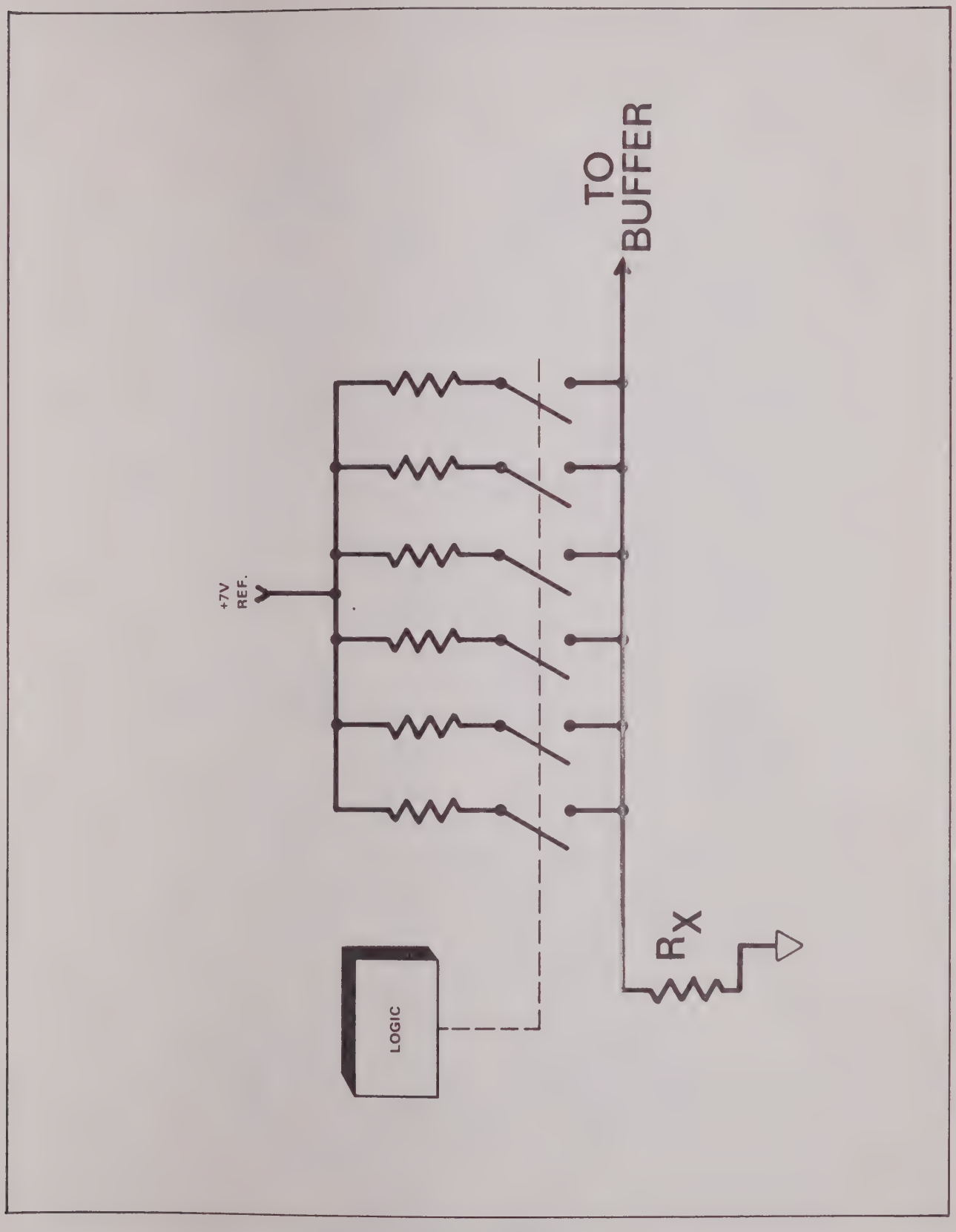


Figure 9. Ω CONVERTER –03

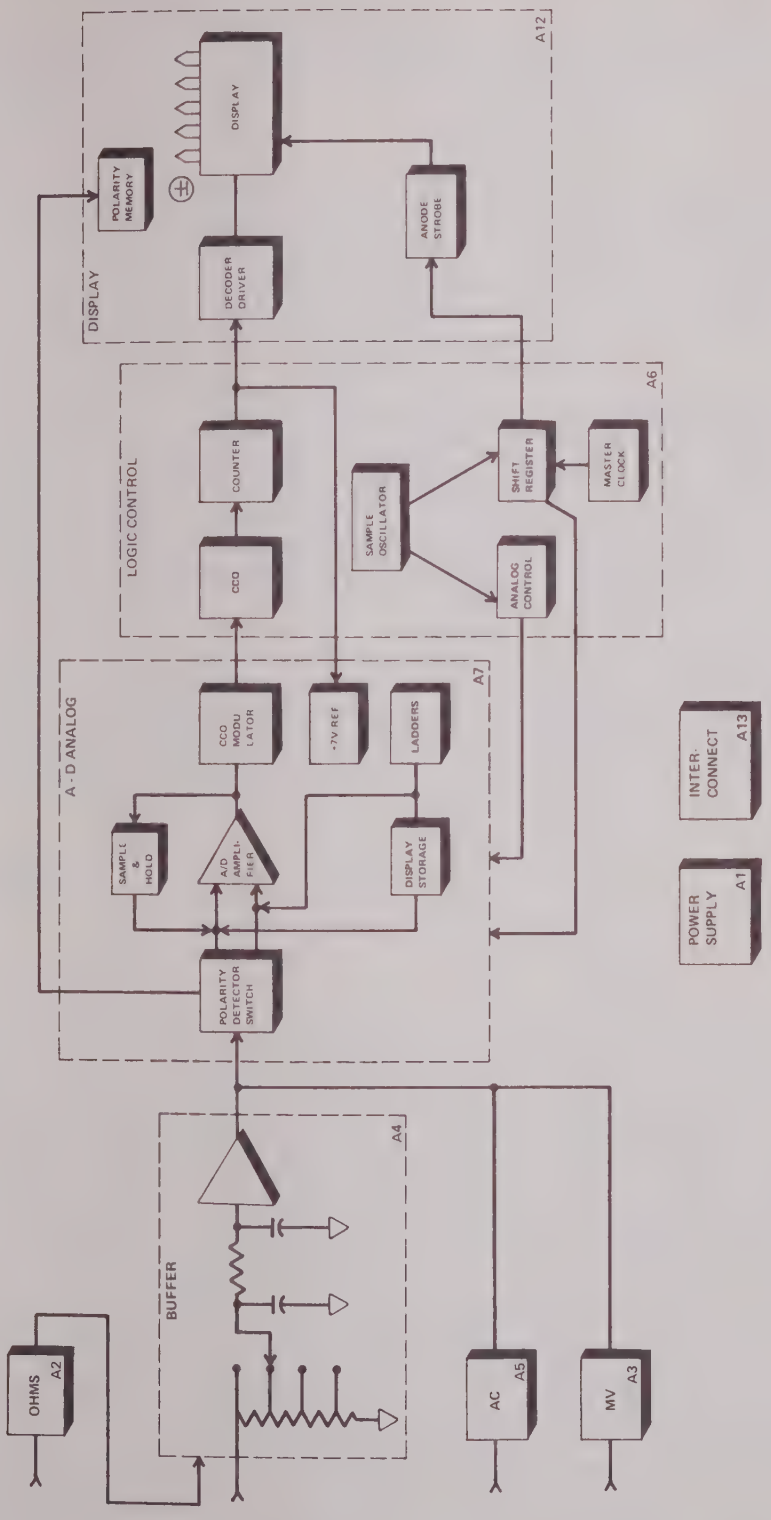


Figure 10. BLOCK DIAGRAM

Note: Since the output of the differential operational amplifier is equal to the difference in input voltage times the gain, the output of the Primary Ladder would cause the output voltage of the A-to-D Amplifier to decrease until it is below 7 volts. When the output of the A-to-D Amplifier is less than 7 volts the CCO Modulator will supply no more current to the Oscillator. The remainder voltage is divided by 7 and is moved into storage in Sample and Hold.

6. The BCD information from the counter being fed to the Decoder Driver translated into decimal format, and as pointed out previously, will cause a ground to occur on the proper numeral line to all of the display tubes. As the count is finished in each time period, the Anode Strobing circuit will cause the proper display tube to light and display the number that has been grounded. The first display tube displays the number digitized in the A time period. The second display tube displays the number digitized in the second or B time period, etc.

7. The output of the A-to-D Amplifier is divided by 7 prior to placing it in Sample and Hold storage. This is the input difference times 10 since the gain of the amplifier is 70, which is divided by 7 before storage. During the second digitizing or B time period, the first remainder is placed on the input of the A-to-D Amplifier, and is digitized and displayed just as was the first digit. Again, the remainder will be stored in another section of Sample and Hold to be used during the third digitizing period. This process is repeated until all four digits have been digitized and displayed.

8. Display Storage functions in such a manner as to receive an analog charge on each of a series of a capacitors representing the digit that was developed in each digitizing period. Though the analog values are stored initially in the Measurement Mode, the output of the Display Storage is used only during the Storage Mode of operation.

THEORY OF OPERATION

TIME

In the Recirculating Remainder system there is an obvious need for time control for Measurement and Storage Modes of operation, in addition to digitizing, display, error removal, and other switching functions that must be carried out in the instrument. Figure 11 is a timing diagram of the time pulses generated in an 8200. The Master Clock output is a 4 kilohertz pulse. This results in one pulse every 250 micro-seconds. Looking at Logic Control schematic (A6), the Master Clock feeds the clock input of the J-K flip-flop U1B, resulting in the F and $\overline{F}$ outputs; a square wave with a 500 micro-second cycle time. Q2, accepting the F signal, produces, at its collector, the $\overline{H}$ signal which is fed to the Shift Register comprising U2A, U2B, U3A, and U3B. Each of the J-K flip-flops in the Switch Register generates one of the digitizing period pulses. The Q output of flip-flop U2A generates the A time output. U2B generates the B time output. U3A generates the C time output. U3B generates the D time output. $\overline{\text{ZERO}}$ is generated by the NAND gate U4B. The inputs to the NAND gate being $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$; when all of these outputs are high, the $\overline{\text{ZERO}}$ pulse is generated. Looking to the right of the schematic diagram, ZERO pulse is generated by the inversion that takes place through Q9. The Sample Oscillator element is CR2, a programmable unijunction transistor which is RC timed and locked in operation with the Master Clock. From the J-K flip-flop U1A, the M or Measure pulse is derived, which is used throughout the instrument for the Measure Mode functions. In the Analog Control circuitry the gate pulses are generated for the various storing and timing functions throughout the instrument.

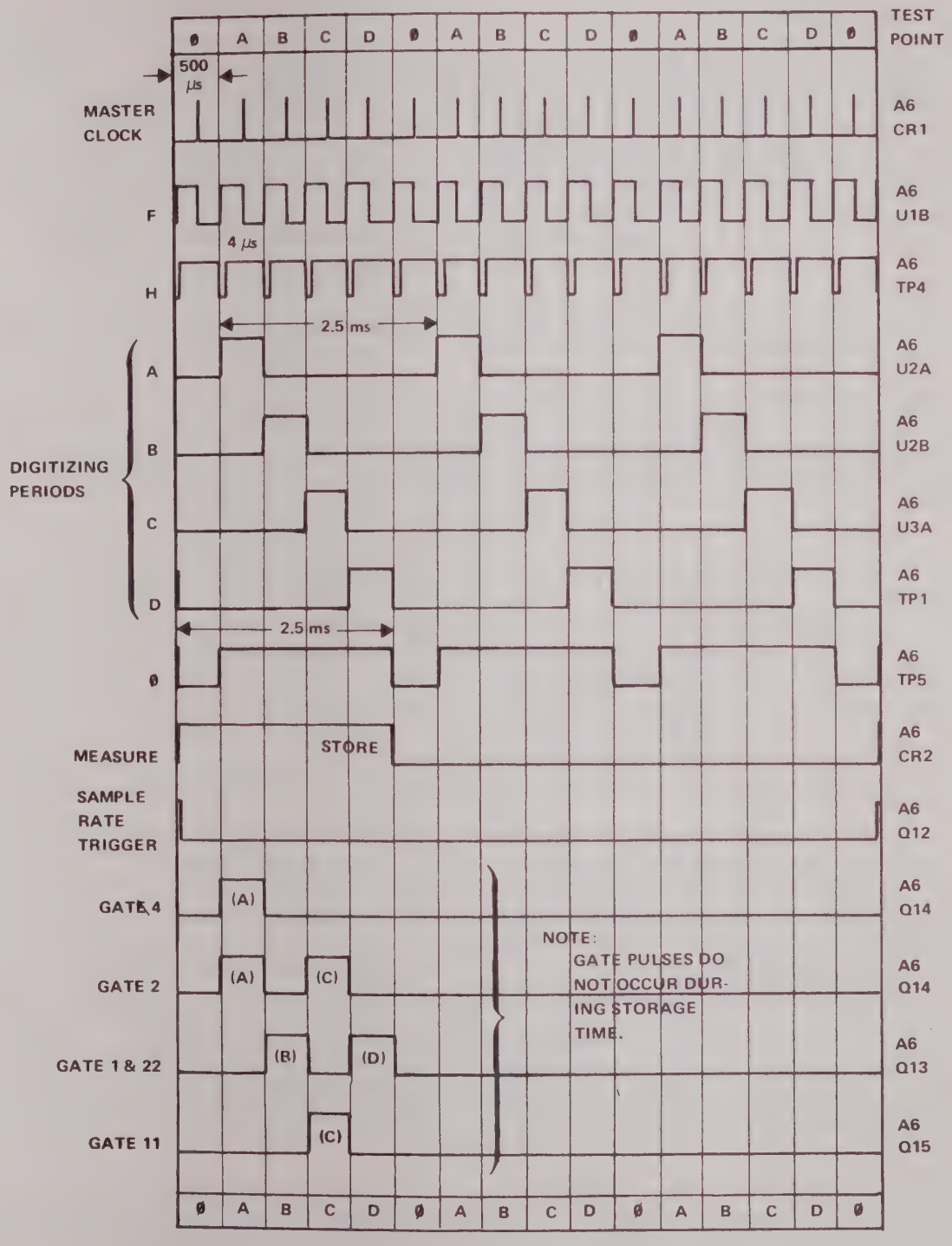


Figure 11. 8200A TIMING DIAGRAM

POWER SUPPLY (A1) Drawing No. 8200A-1001

Voltages from the A17 Transformer assembly are fed to each of three bridge rectifiers. Starting with the regulated +15 volt DC supply, 36 volts AC is applied from the power transformer across the rectifier bridge composed of CR5 through CR8. The positive side of the bridge is fed through R6 and Q3 as the series pass element. It is referenced to the Zener diode CR9. The +15 volt power supply is used as the reference voltage for the other three supplies. Reference for the minus 15 volt supply is developed as a result of the voltage division through R14 and R18 between the plus and minus 15 volt supplies. R21 connects the 5 volt supply back to the 15 volt supply for reference. The 200 volt display supply is connected back from the collector of Q2 to the 15 volt supply; the base of Q2 being connected to the voltage drop between R3 and R4 and is referenced in that manner.

BUFFER (A4) Drawing No. 8200A-1004

The overall gain of the Buffer is 1 inverted, and the Buffer serves five separate functions: an Input Divider, an Active Filter, Overload Protection, the Buffer Amplifier, and the Logic circuitry.

The Input Divider offers an input impedance of 10,000 meg ohms shunted by less than 130 pf, and in the 10 to 1000 volt ranges offers an input impedance of 10 meg ohms. Monolithis amplifier U1 serves as the active element in the filter. K6 closes to activate the filter, which provides 60 db at 50 hertz and 100 db at 200 hertz and above. CR25 and CR26 serve as protection diodes and rapid overload recovery, while CR23 and CR24 protect the filter amplifier.

Overload protection has been provided that operates at a 2 volt level as provided by CR1, CR2, Q6, and Q7. They operate with 1.4 volts on the base and .6 volts on the emitter, and serve to keep U2 and the U3, the Buffer Amplifiers, in linear operation. VS1, a neon bulb, holds the input potential below 100 volts and indirectly illuminates the readout portion of the front panel. CR3 and CR4, at the output of the Buffer Amplifier, serve function as a fast feedback for over voltage,preventing saturation in the amplifier. The amplifier itself being a differential input operational amplifier with a total gain of 1 and composed of dual FET U2 and monolithic amplifier U3.

A-TO-D ANALOG ASSEMBLY (A7) Drawing No. 8200A-1007

Seven separate circuits make up the A-to-D Analog Assembly: the Polarity Detector, A-to-D Amplifier, CCO Modulator, Sample and Hold circuit, Ladder circuit, Display Storage, and +7 volt Reference Supply. The Polarity Circuit consists of three transistors, Q13, Q14, and Q15, which operate the polarity switches consisting of FET's Q10, Q12, and Q16. The Polarity Detector is enabled by the pulse GATE 4 at Q13. GATE 4, consisting of A time, and Measure Mode, is generated in the Logic Control assembly A6. A negative voltage appearing on R15 will cause Q14 to conduct. The line P from the emitter of Q14 will go high, and Q10 and Q16 will conduct. If, in contrast, the voltage on R15 is positive, Q15 will conduct, $\overline{P}$ from the emitter of Q15 will go high and Q12 will turn ON. The voltage on R15 is opposite in polarity to the input of the instrument due to the inversion in the Buffer. The P and $\overline{P}$ signals are used in the Display circuit to indicate polarity. If $\overline{P}$ is high, positive voltage is being fed to the 8200. If P is high, negative voltage is being fed to the 8200.

The A-to-D Amplifier consists of a dual FET, U3, and a monolithic amplifier U2. The overall gain of the amplifier is 70, and its normal input is from zero to 1.6 volts. It is connected as a differential input operational amplifier. Offset removal is accomplished with C7 and FET switches Q16 and Q20. During the ZERO time period Q16 and Q20 conduct placing C7 in the output of the A-to-D Amplifier. When the ZERO pulse is completed, Q16 and Q20 open, C7 is effectively placed in series with the amplifier. Q16 functions to short the input of the A-to-D Amplifier, and Q20 functions to connect C7 to a 1 to 69 divider in the A-to-D Amplifier output. In this manner, offset is removed from the A-to-D Amplifier.

Q19 and Q21 provide a fast feedback circuit to prevent the amplifier from saturating. Such precautions are necessary, in that an operational amplifier once saturated generally takes several seconds to recover. Q11, in the input circuit of the Amplifier, is a temperature compensation device.

The CCO modulator, or constant current oscillator modulator, operates to produce current from the emitters of U26 and U30 to operate the constant current oscillator. When the output of the A-to-D Amplifier is above 7 volts, the modulator is caused to supply current. Q26 supplies the high current during large voltage outputs, and the differential pair Q27 and Q28 control Q29 and Q30 to supply current when the output approaches 7 volts. R48 adjusts the activation point of Q27.

Q22, Q23, Q24, and Q25 are connected to gate pulses that appear only during Measure Mode. In the block diagram explanation it was pointed out that Sample and Hold operates only during the Measure Mode. Capacitor C9 stores the remainder in the A time period. No remainder is stored in the D time period.

The Primary and Secondary Ladders are caused to operate by a single set of Ladder Switches composed of Q31 through Q42. Q39 through Q42 accept the $\overline{W}$, $\overline{X}$, $\overline{Y}$, and $\overline{Z}$ information from the BCD Counter and translate the BCD information into ladder switching. The Primary Ladder is composed of R55, R57, R59, and R61, plus R52 and R53 which serve as calibration resistors. The Secondary Ladder is composed of R54, R56, R58, and R60. In addition, R51 and R74 add one-half digit of bias for the Display Storage to compensate for possible leakage. The output steps of the ladder are in Binary Coded Decimal 8421 format. The output of the Primary Ladder feeds the input of the A-to-D Amplifier. The output of the Secondary Ladder feeds the Display Storage circuitry.

As was covered in the block diagram description, Display Storage is used in Storage Mode only. Display Storage consists of Q4 through Q9. Q4 is enabled by the STORE IN pulse which occurs during the last half of each digitizing period, and provides a path from the Secondary Ladder to the storage capacitors C3 through C6. The analog value representing the numbers that have been digitized are stored in these four capacitors.

The STORAGE OUT pulse on the gate of Q9 occurs only during the Storage Mode.

During Measure Mode analog values are placed in storage, since STORE IN and each of the store A, B, C, and D pulses occur. None of the voltages are taken out during Measure Mode, since the STORAGE OUT pulse on the gate of Q9 does not occur in Measure Mode.

In Storage Mode the STORAGE OUT pulse occurs and connects storage capacitor C3 to the input of the A-to-D Amplifier. After the first digit is digitized the voltage is restored during the last half of the time period by the STORE pulse enabling the gate of Q4. Each increment stored on the capacitors is digitized and the analog value restored on the respective capacitors in a similar manner.

+7 Volt Reference Supply

The +7V Reference Supply is fed power by the +15V Supply and referenced to a zener pack U1. R7, R8, and R9 form a voltage divider for the adjustment of the +7V. R75 protects Q1, the series pass element, from short circuits, and the +7V DISABLE, when grounded, removes the drive of Q1 disabling the +7V reference supply. This is done in order to feed the instrument with External Reference Voltage.

LOGIC CONTROL (A6) Drawing No. 8200A-1006

Master Clock

The Master Clock, composed of CR1 and Q1, is an RC control generator operating at approximately 4 kHz, and can be reset by the Data Output option or the Printer Output option producing a pulse on the Master Clock reset line, which connects to the emitter of Q1. The output of the Master Clock is applied to J-K flip-flop U1D. The outputs of U1D carry the F and $\overline{F}$ pulses. Referring to Figure 11, the relationship between Master Clock pulses and the remaining pulses generated in the Logic Control assembly can be seen. The F pulse is applied to the base of U2, and from the emitter of U2 we generate the $\overline{H}$ pulse which is applied to the Shift Register.

Shift Register

Four J-K flip-flops in series U2A, U2B, U3A, and U3B form the Shift Register, which divides the H pulses and produces the four digitizing period time pulses A, B, C, and D. $\overline{ZERO}$ pulse is generated by feeding the outputs of the Shift Register to a NAND gate U4B, and the ZERO pulse is generated by the inversion created by feeding $\overline{ZERO}$ to the base of Q9. The Shift Register may be reset by the Shift Register reset line which is connected to the four flip-flops in the Shift Register and to the set line of U1D.

Sample Oscillator

The Sample Oscillator is a programmable unijunction transistor CR2, which is RC timed by R13 and C3 and operates at a 4 kHz rate. The Sample Oscillator can be keyed by the Sample Oscillator pulse line. The output of the Sample Oscillator is fed to the J input of a J-K flip-flop U1A. The ZERO pulse is connected to the clock input of that same flip-flop. This causes the Measure Pulse or impulse to be generated at the start of ZERO time.

Analog Control

The Analog Control circuits generate the Store A, Store B, Store C, and Store D pulses, which are used in the A-to-D Analog Module. The Shift Register $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$ pulses are connected to the bases of Q5 through Q8. Their emitters are connected back to the Shift Register reset line so the Analog Control Store pulses are disabled during the reset pulse.

Current Controlled Oscillator

The Current Controlled Oscillator, which is the multivibrator formed by Q3 and Q4, receives its current input from the CCO modulator in the A-to-D Analog Assembly, and supplies a pulse train when it receives current. The pulse output is proportional to the current being fed to the multivibrator. The higher the current being fed, the higher the pulse rate. The Current Controlled Oscillator is enabled by the F pulse and held disabled during the $\overline{H}$ time or reset period. This enables the Current Controlled Oscillator during the first half of each digitizing period after the reset pulse is completed.

Counter

Four J-K flip-flops make up the BCD Counter formed by U5A, U5B, U6A, and U6B. The Z, Y, X, and W outputs of the Counter are shown on the 16 state Binary Counter table shown in Figure 12, the Z output representing a binary 1, the Y output a binary 2, the X output a

binary 4, and the W output a binary 8. The NAND gate U4A is the up-ranging element in the system, generating a UP signal when Z, Y, X, and W are all high. The down-range signal is generated by U8B when Z, Y, X, and W are all low. The UP and DOWN signals are fed to the Interconnect assembly where the additional qualifying pulses. Measure and time period A, are added in order to enable autoranging only during the A time period of Measurement Mode.

STORE IN, STORE OUT, and gate pulses are generated in the logic control assembly by the action of Q10 through Q15 and NAND gates U7A, U7B, U7C, and U7D.

DISPLAY (A12) Drawing No. 8200A-1012

Numbers are displayed in sequence. The A time period displays the most significant digit. The B time period displays the second most significant digit, etc. until all four digits have been displayed. The A digit includes over-ranging to 15 and each digit is displayed only during the last half of its respective time period. During the ZERO time period none of the display tubes are on.

Anode Strobing

Looking at display assembly schematic A12, when the F signal is low, which occurs during the last of each digitizing period, it enables transistors Q5, through Q8, which completes one-half of the ON path for each of those transistors. The other half of the ON signal for those transistors consists of the digitizing pulses applied to their bases. For example, the digitizing A pulse being applied to the base of Q5 will turn Q5 ON during the A time period when F is low. This occurs during the last half of the A time period and Q5 will conduct causing Q1 to conduct and apply the 200 volt ionizing voltage to the anode of DS3 which will cause any number to ionize which has been grounded by U1, the Decoder Driver.

Polarity Memory

CR6 and CR7 operate as a NOR gate. If VDC or MV are selected the VDC CONTROL or MV CONTROL line will go low enabling Q13 and Q14. The P and the $\overline{P}$ signal lines carry the polarity information from the A-to-D amplifier assembly detector. If P is high a negative voltage is being fed into the 8200A. If $\overline{P}$ goes high a positive voltage is fed into the instrument. The signals P and $\overline{P}$ last only during the A time period of Measurement Mode. The P signal will turn on the gate of Q15 causing it to conduct and causing the multivibrator, formed by Q13 and Q14, to flop to a condition wherein the potential on the collector of Q13 will cause a low voltage on the minus sign in DS1 which will be pulsed on during the B time period when Q6 has turned on by the base signal on its base and the F signal on it's emitter. This conduction will cause Q18 to conduct and allow the 200 volts to be applied to V1. The polarity memory circuit is a flip-flop formed by Q13 and Q14 that remains in which ever state it was pulsed to last.

Decoder Driver

Decoder Driver U1 translates the BCD coded information on the W, X, Y, and Z lines which are inverted by inverters U2A, U2D, U2E, and U2F into grounds on the appropriate lines to all the display tubes. It should be noted that this is a 16 state Counter and care should be taken if any attempt is made to substitute this decoder driver, in that most decoder drivers count to 9 or 10, consequently substitution can lead to problems in the 8200.

Lamp Assembly

A small printed circuit board mounted on the display assembly contains the POWER, REMOTE, EXT REF, and FILTER switches plus two indicator lamps indicating filter selection and external reference selection. This assembly also carries the Millivolt ZERO potentiometer which is connected between +5 and −15 volts and is mounted on this board so that it may be adjusted via a hole in the front panel.

INTERCONNECT (A13) Drawing No. 8200A-1013

Function Command

When the 8200 is in local control a ground is furnished on J12 Pin 30 which is series connected through all six function switches. In addition, the function switches are mechanically interlocked to prevent operation of more than one switch at a time. If the REMOTE switch is operated no ground is furnished to pin 30 and the functions will be controlled from the Remote Control Assembly (A8).

Range Command

A ground signal is series connected through the Range Command switches which supply the $\overline{Ra}$, $\overline{Rb}$, $\overline{Sa}$, and $\overline{Sb}$ lines which control the Range Register.

Range Register

U1A and U1B are J-K flip-flops with outputs of a, $\overline{a}$, b, and $\overline{b}$, the range control signals. Range code is given in Figure 12. These range code signals are generated when the instrument is in both manual and autoranging and are fed to each input circuit to control the relays in that circuit.

As was pointed out in the Logic section $\overline{UP}$ and DN signals are generated when the count from the BCD counter reached 15 for a $\overline{UP}$ signal or was ZERO to generate a DN or down signal. These signals being fed to the Range Register through additional signal qualifiers will only cause a range change when the clock input to U1B or U1A, the $\overline{MaF}$ signal, is available which occurs only during Measurement mode in the A time period when the F signal is high. So ranging can occur only in Measurement mode in the A time period.

MILLIVOLT CONVERTER −02 OPTION (A3) Drawing No. 8200A-1003

The Millivolt Converter consists of an operational amplifier with a dual gain of 10 or 100 and feeds the A/D Analog assembly in the 8200. This makes possible ranges of 100 millivolts and 10 millivolts. The output range of the Millivolt Converter is ZERO to 1.6 volts and it contains A3 pole filter. The input of this amplifier consists of a dual transistor U7 which gives excellent temperature and bias characteristics in addition to a very low noise input. The Millivolt Converter also contains its own logic for autoranging, including the DC ranges. U6 is a monolithic operational amplifier with both low bias and low drift and whose output drives Q5 or Q6 to provide polarity spreading in the output and increase the current drive.

K1 closes whenever the millivolt function is selected. This connects the high terminal to the amplifier and provides a connection for the low terminal to signal common. K3 selects the output range of the instrument. With K3 closed the instrument is in the 100 millivolt range as determined by the feedback resistance. The Millivolt ZERO is adjusted by R15 which can be adjusted through

an access hole in the front panel of the instrument when the Millivolt Converter is installed. R13 adjusts the millivolt bias current.

Overload protection is provided by CR1, CR2, CR3, and CR4. Current can be conducted through CR1 or CR2 and through R28 or R29 back to the LOW terminal in overload conditions. Similarly, current may be conducted through R3, R4, CR3, CR4, and R19. The output of the amplifier is limited by R20 and R21. These resistors limit the maximum current available to R23.

When the millivolt option is installed, the MV SENSE RANGE line is automatically connected to logic common. This defeats the VDC control command on the Buffer board. The new VDC control and MVDC control are both on the millivolt board. .There is a 2 state flip-flop comprised of U4A and U4D which selects either the millivolt or the volt DC range when either the $\overline{\text{MVDC}}$ CONTROL or $\overline{\text{VDC}}$ CONTROL is low. The autorange and logic is provided by U1A, U2C, U3B, and U3A. When the Millivolt Converter is installed, the function lights associated with the Millivolt Converter operate, in that all of the interconnect wiring is already accomplished in the basic instrument.

AC CONVERTER –01 OPTION (A5) Drawing No. 8200A-1005

The AC Converter is composed of two basic circuits plus logic. An operational rectifier which is composed of Q1, a voltage follower used to reduce the capacitance and increase the input impedance, Q3 and Q4 a differential pair for current supply, Q2 and Q5 which supply the bias current to make the clipping symmetrical, and Q6 which compensates for the diode capacity while CR7 and CR8 provide protection for Q3 and Q4. Feedback switching is used in the amplifier to accomplish range switching.

The operational rectifier is followed by a DC difference amplifier with about 2 ma of output at full-scale. It includes RC filtering and spreading diodes CR13 and CR14 to enhance the polarity signal. U3 is a monolethic operational amplifier that has been selected for its low drift characteristics.

$\overline{\text{VAC}}$ CONTROL line will activate K1 and K2. Range code information into U1A, U1B, U1C, and U1D provide the necessary drive signals for K3, K4, and K5, the ranging relays.

The input is capacitively coupled through C1 to R1 and C2 in parallel combination. Q1 is a voltage following amplifier whose function is to reduce the input capacity and increase the input resistance of the amplifier. Q2 is a differential amplifier with one input capacitively coupled to Q1 while the other input is coupled to ground. The output of this differential amplifier is applied to the differential pair Q3 and Q4. Q2 biases this differential pair. Q5 is used to bias the differential amplifier U2 and control the level of the collector of Q4. The level determines the symmetry of the circuit. R31 is the symmetry control. CR11 and CR12 in conjunction with the amplifier operate as an operational rectifier. The output of these two diodes is passed through a DC difference amplifier integrator. The output of these diodes is roughly divided by 10 either by R34, R35, or R36 and R35 which forms the output voltage dividers. The signal on R35 is then fed back through the range determining feedback resistors to the summing junction which is the gate of Q1. R16 and R23 constitute the resistive feedback for the 1 volt range. R17 and R24 constitute the resistive feedback for the 10 volt range. R18 and R25 are the feedback circuit for the 100 volt range and R19 is used as the feedback resistor for the 1000 volt range. Feedback capacity for the 1 volt range is composed of C11 while C12 and C15 serve the same function for the 10 volt range and C13, C16, and C17 form the capacity feedback for the 100 volt range and C18 is the feedback capacity for the 1000 volt range. These capacitors compensate for the capacity of C2 in the input.

The DC difference amplifier takes the difference between the positive and negative signal, rectifies sign waves, averages them, and produces a DC output. Spreading diodes CR13 and CR14 serve as a convenience for the polarity sensing to insure the proper polarity into the A-to-D amplifier.

ZERO control is provided by R48 and the associated circuitry of R47 and R44. U3 is a selected low drive amplifier with an overall gain such that a 1 volt peak sign wave input will result in .707 volts of output. Thus, the output represents the RMS voltage. However, it is average responding. Adjustment of the overall gain is accomplished with R46, then each range is adjusted in sequence. Adjustment and calibration order is given on the inner guard cover on the instrument which must be in place when the instrument is calibrated.

Ohms Converter —03 Option

The Ohms Converter operates in such a manner as to use the 7 volt reference as the source of current flow through the unknown resistance to be measured. The 8200 then measures the voltage drop across the resistor thus providing a direct measure of the voltage across the resistor with a known current. The 10 MΩ range is activated through dividers R1, R2, and R3 in combination with R5, R1 being the calibration adjustment. The divider reduces the voltage on R5 to only .7 of a volt. This eliminates having to have a 70 megohm resistor from the 7 volt supply directly to the INPUT HI.

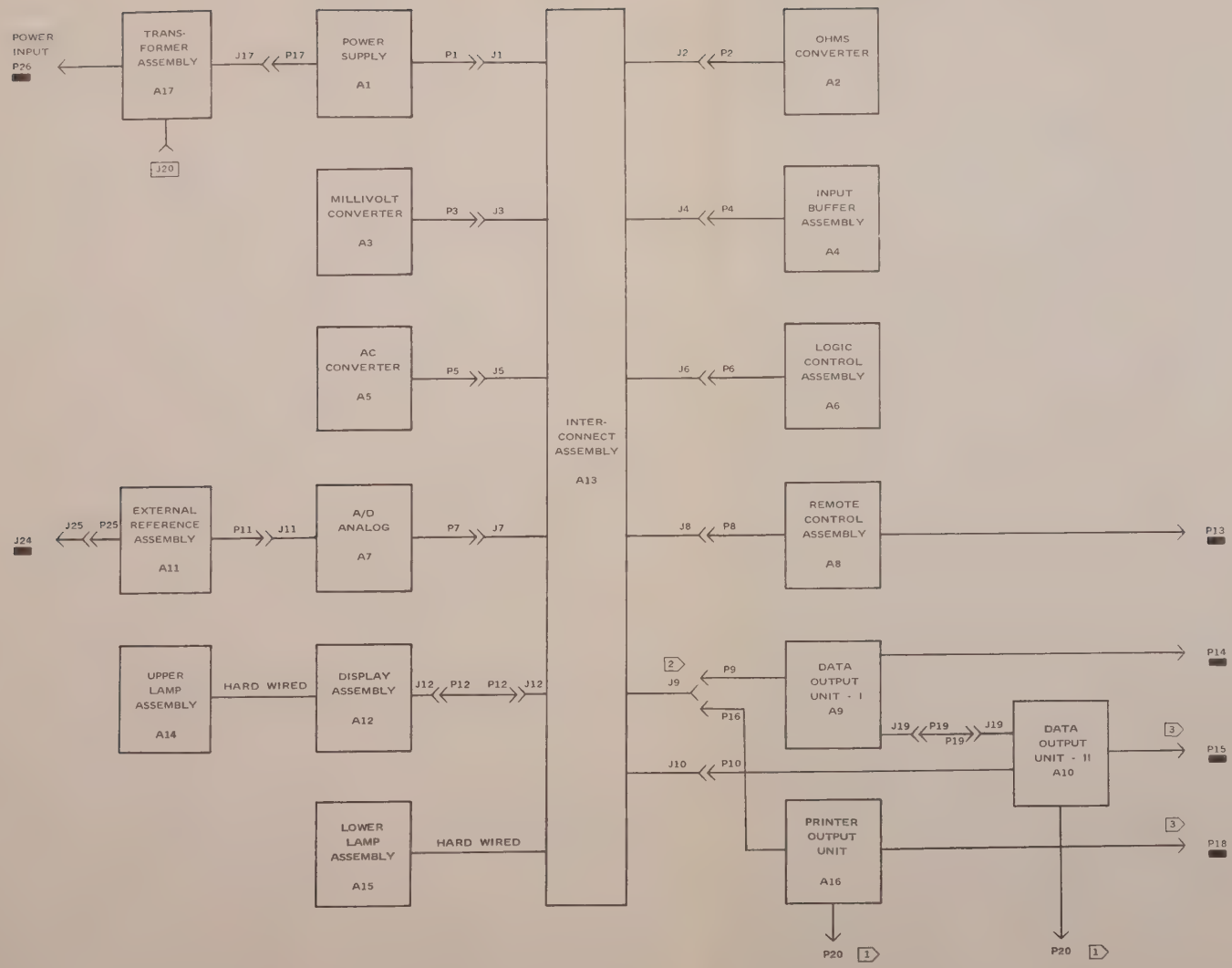
The 1,000 KΩ range is called when K1 is closed. This puts 7 volts across R5 increasing the current from 100 picoamps which was used in the 10 MΩ range to 1 microamp. R4 is the calibration adjustment to this range. The 100 KΩ range is called when both K1 and K2 are operated. R6 and R7 provide an additional 9 microamps making the total current 10 microamps. R6 is the calibration adjustment for this range. The 10 KΩ range is called when K3 is operated. R8 and R9 provide 100 microamps through the resistance to be measured. K8 being the calibration adjustment. The 1 KΩ range is called by operating K3 and K4. R10, R11, and R27 provide an additional 900 microamps or a total of 1 milliamp through the unknown resistance. R10 is the calibration adjustment for the 1 KΩ range. The 100 ohm range is called by operating K5. R12, R13 and R15 provide 10 milliamps of current through the unknown resistor. R12 being the calibration adjustment.

F1 is a fusible link with a current capacity of 100 milliamps. It is activated whenever an overload voltage of greater than 30 volts is applied between HIGH and LOW; CR1 and CR2 together with CR20 and CR21 constitute overload protection dials. CR1 and CR2 are 10 volt zeners while CR20 and CR21 furnish a return path current to INPUT LOW. When excessive voltage is applied to INPUT HIGH, current will flow through range resistors and CR2 or through R14 and CR1. This prevents the input voltage from overpowering the 7 volt supply and destroying parts of the A-to-D Analog circuitry. If voltage greater than 130 volts is applied to the KΩ range, R11 will overheat and possibly be destroyed. No damage will result in the A-to-D Analog assembly.

An Ohms function can be commanded by the $\overline{\Omega}$, $\overline{K\Omega}$ or $\overline{M\Omega}$ CONTROL lines which drive Q3, Q4 or Q5. When the $\overline{AR}$ line is high indicating that a valid range has been called, either Q3, Q4, or Q5 will be ON depending upon which control line is low. The collectors of these transistors are connected through diodes CR13, CR14, and CR15 to reset lines of 3 state flip-flop comprised of U5B, U3A, and U3B.

Transistors Q3 through A5 and Q8 through Q10 plus NAND gates U3A, U3B, and U5A combine to command the required functions. NAND gates U4A through U4D plus transistors Q6 and Q7 control the range in the KΩ function. NAND gates U1A, U1B, U2A, and

U2B provide the autoranging gate signals. NAND gate U2D provides a delayed MΩ relay line for the autorange logic on the A13, Interconnect assembly. NAND gate U2C provides a delayed $\overline{\text{OHM}}$ relay line for logic on the Interconnect assembly. The Ohms Converter Option is the only input option that feeds the 8200 Buffer assembly. All other input options feed directly to the A-to-D Analog assembly.



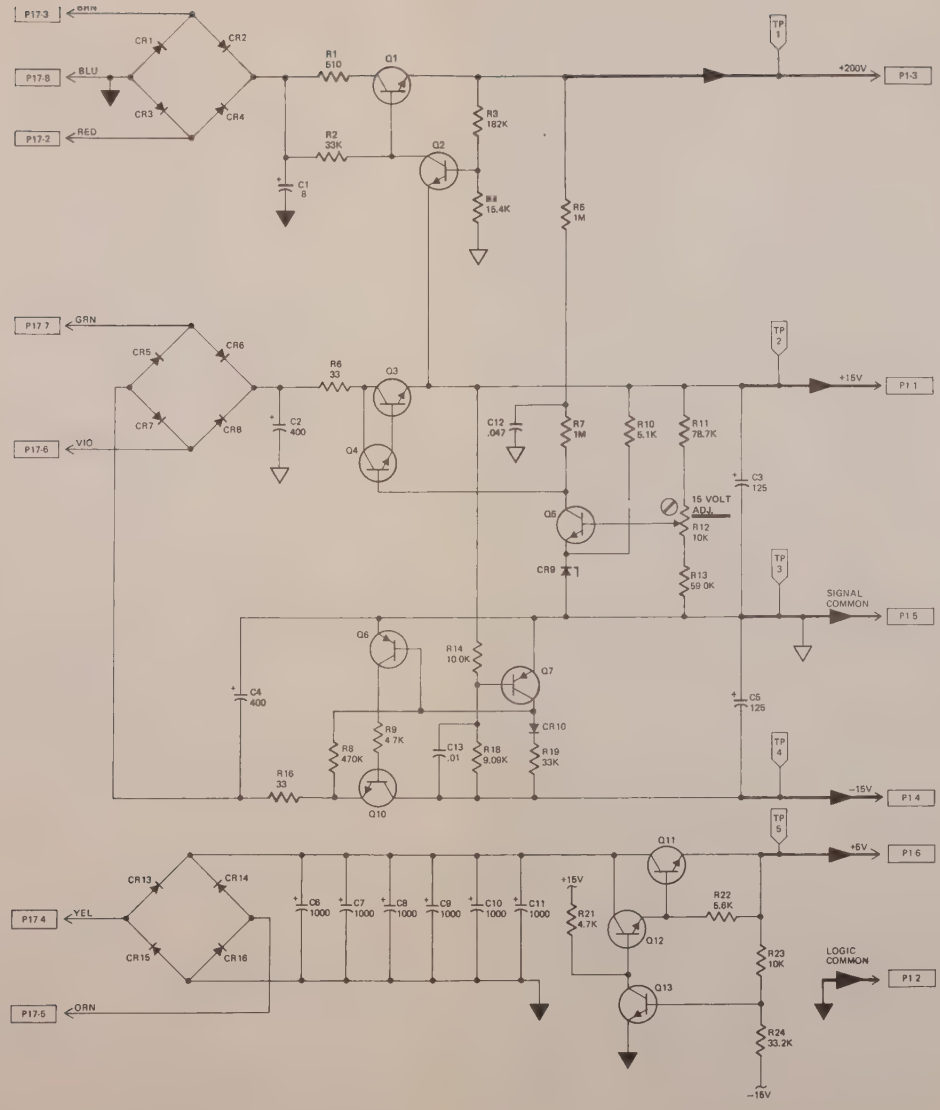
LIST OF SCHEMATICS AND DIAGRAMS

NAME	ASSY. NO.	SCHEM. NO.
ASSEMBLY INTERCONNECT DIAGRAM	NONE	1
POWER SUPPLY	A1	2
OHMS CONVERTER	A2	3
MILLIVOLT CONVERTER	A3	4
INPUT BUFFER ASSEMBLY	A4	5
AC CONVERTER	A5	6
LOGIC CONTROL ASSEMBLY	A6	7
A/D ANALOG	A7	8
REMOTE CONTROL ASSEMBLY	A8	9
DATA OUTPUT UNIT — I	A9	10
DATA OUTPUT UNIT — II	A10	11
EXTERNAL REFERENCE ASSEMBLY	A11	12
DISPLAY ASSEMBLY	A12	13
INTERCONNECT ASSEMBLY	A13	14
PRINTER OUTPUT UNIT	A16	15
WIRING DIAGRAM AND INPUT POWER SCHEMATIC	NONE	16

NOTES:

1. ▬ DENOTES REAR PANEL CONNECTOR.
2. [1] MATES WITH A17J20 FOR +5V LOGIC SUPPLY INPUT POWER: CONNECTIONS FOR ONE ASSEMBLY ONLY, EITHER A10 OR A16.
3. [2] EITHER A9P9 OR A16P16 MATES WITH J9, SINCE DOU AND POU OPTIONS ARE MUTUALLY EXCLUSIVE.
4. [3] P18 AND P15 SHARE THE SAME REAR PANEL LOCATION.

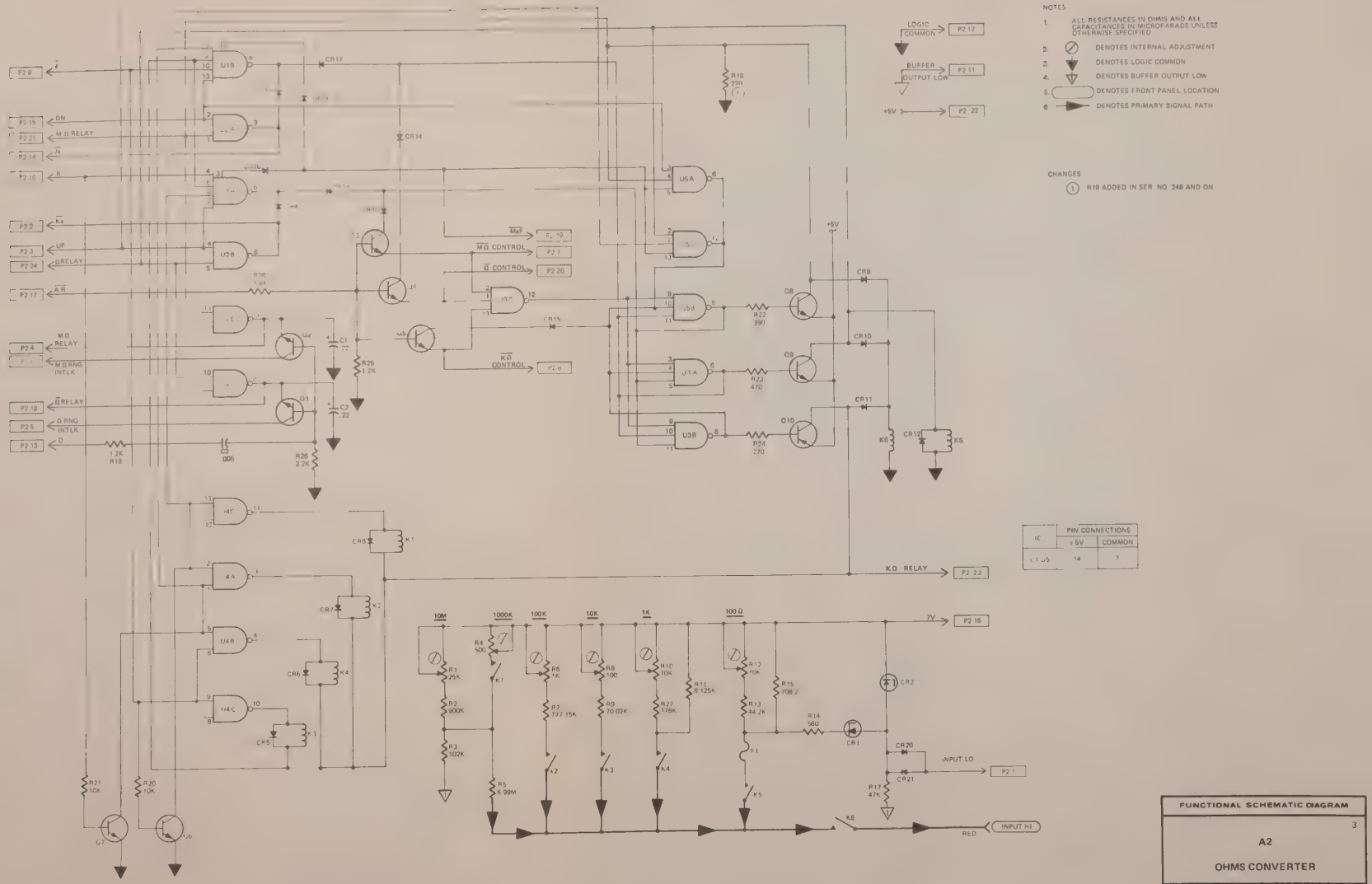
INTERCONNECT DIAGRAM	
ASSEMBLY INTERCONNECT DIAGRAM	1
DRAWING NO. 8200A-1100	REV —
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT
3. ▼ DENOTES LOGIC COMMON.
4. ▽ DENOTES SIGNAL COMMON
5. ——▶—— DENOTES PRIMARY SIGNAL PATH.

FUNCTIONAL SCHEMATIC DIAGRAM	
A1 POWER SUPPLY	2
Drawing No. 8200A-1001	REV a
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



FUNCTIONAL SCHEMATIC DIAGRAM

3

A2

OHMS CONVERTER

Drawing No. 8200A-1002

REV. —

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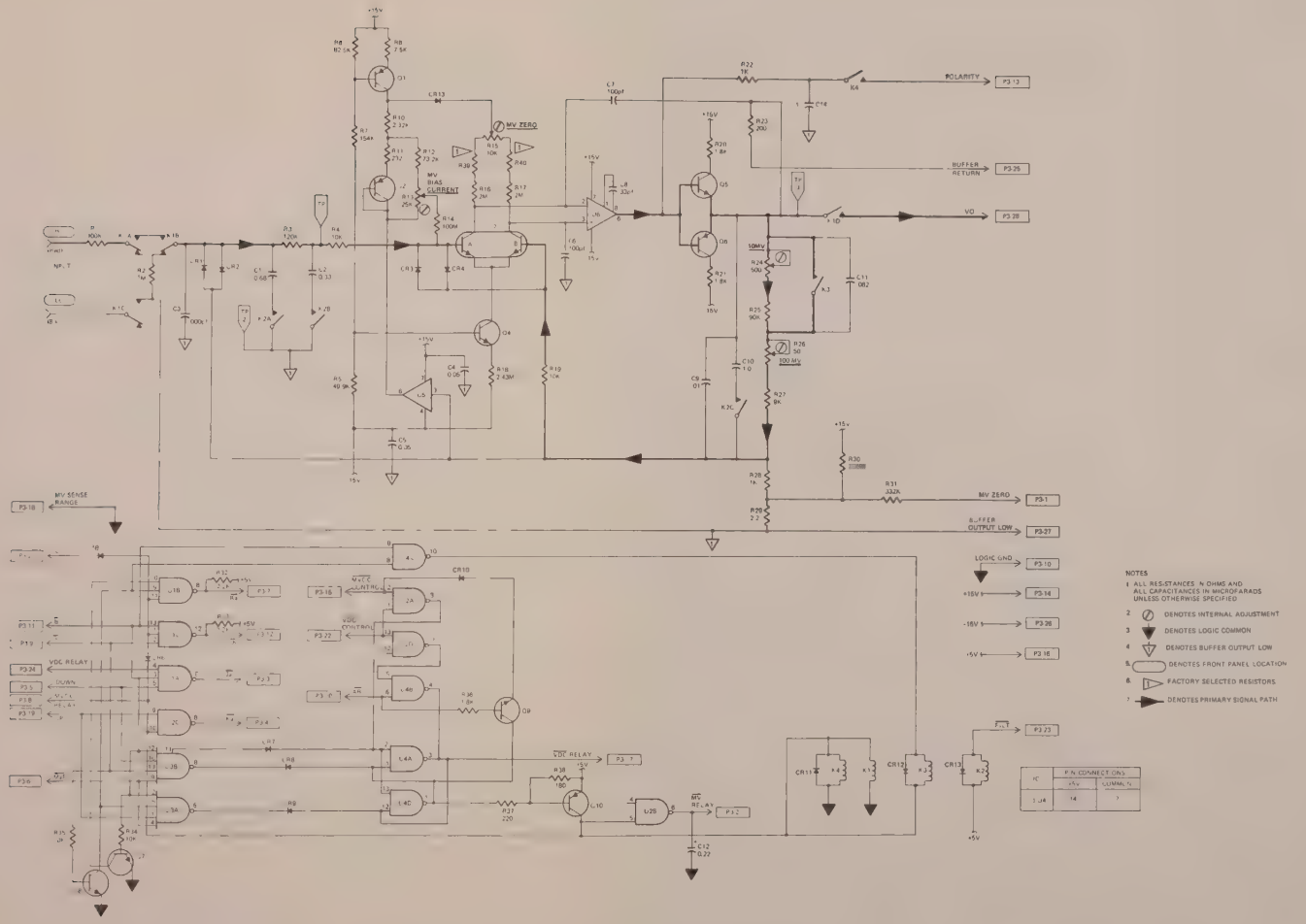
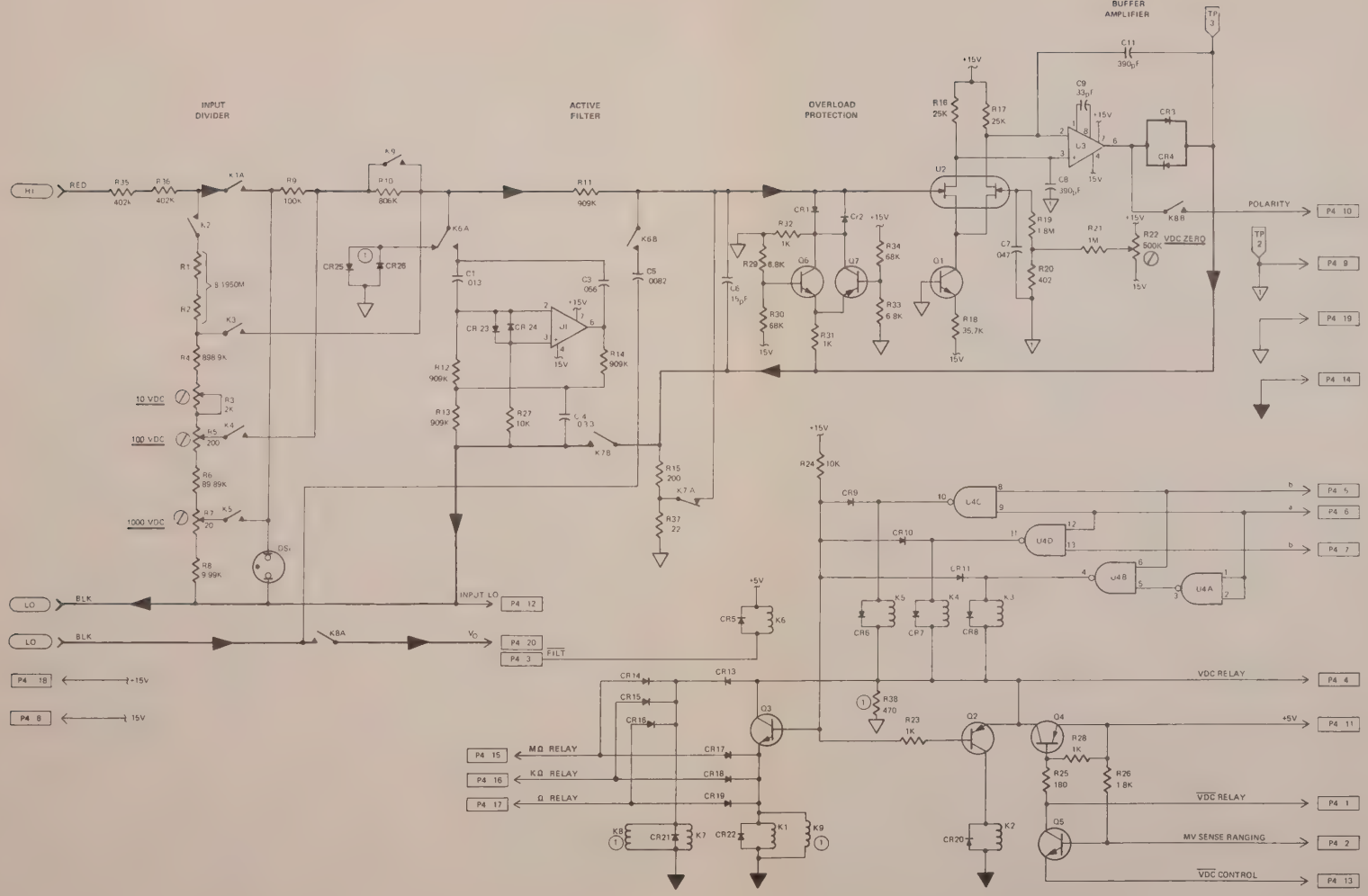
P O Box 7428 Seattle, Washington 98133



FUNCTIONAL SCHEMATIC DIAGRAM	
	4
A3	
MILLIVOLT CONVERTER	
Drawing No. 8200A-1003	REV —

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT
3. DENOTES BUFFER RETURN
4. DENOTES BUFFER OUTPUT LOW
5. DENOTES FRONT PANEL LOCATION.
6. DENOTES LOGIC COMMON
7. DENOTES PRIMARY SIGNAL PATH.

CHANGES

(1) R38, CR26, CR26, K8 and K9 added in Ser. No 329 and on

IC	PIN CONNECTIONS	
	+5V	COMMON
U4	14	7

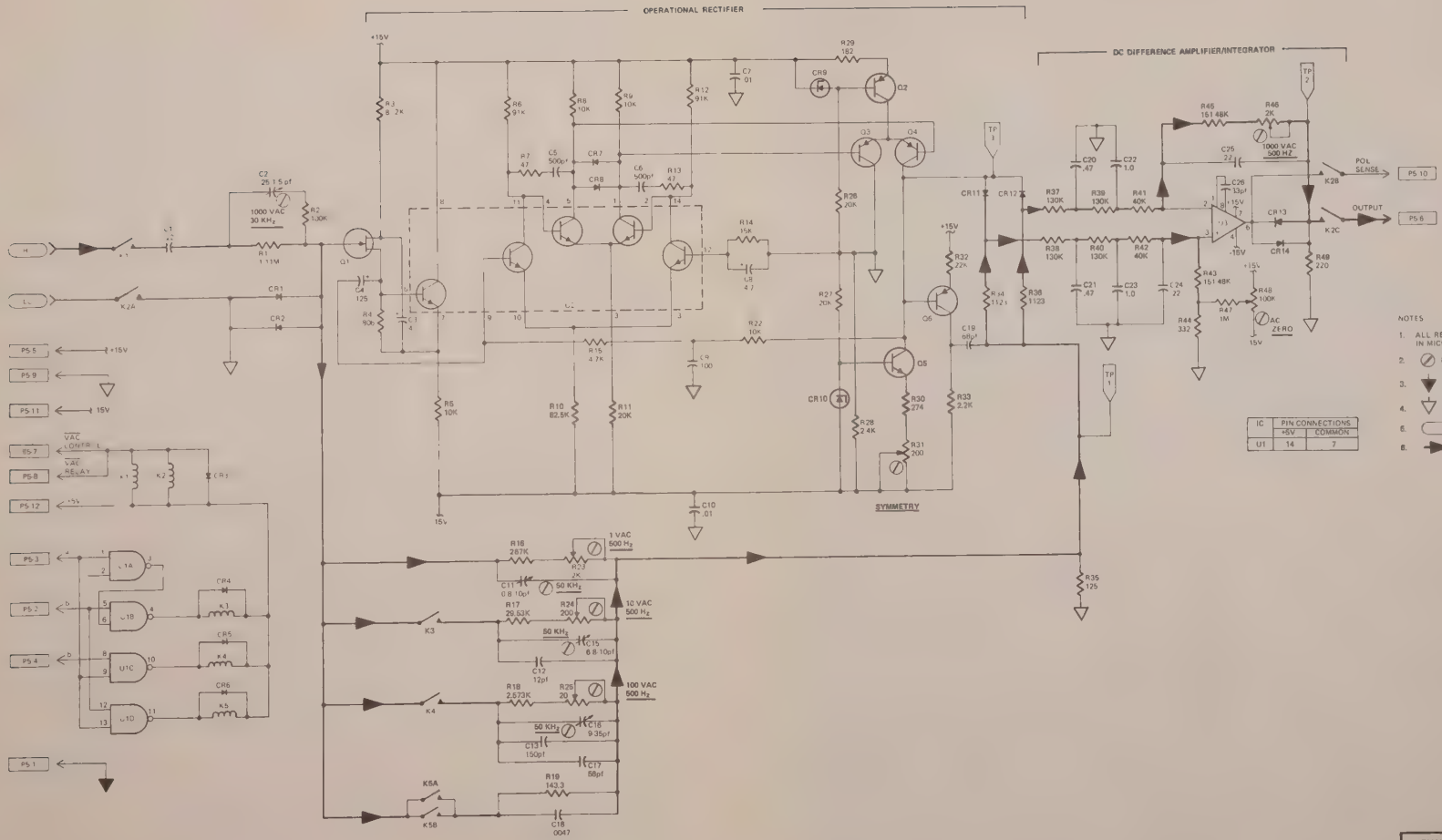
FUNCTIONAL SCHEMATIC DIAGRAM

5

A4
INPUT BUFFER ASSEMBLY

Drawing No. 8200A-1004 REV —

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



FUNCTIONAL SCHEMATIC DIAGRAM

6

A5

AC CONVERTER

Drawing No. 8200A-1005 REV. —

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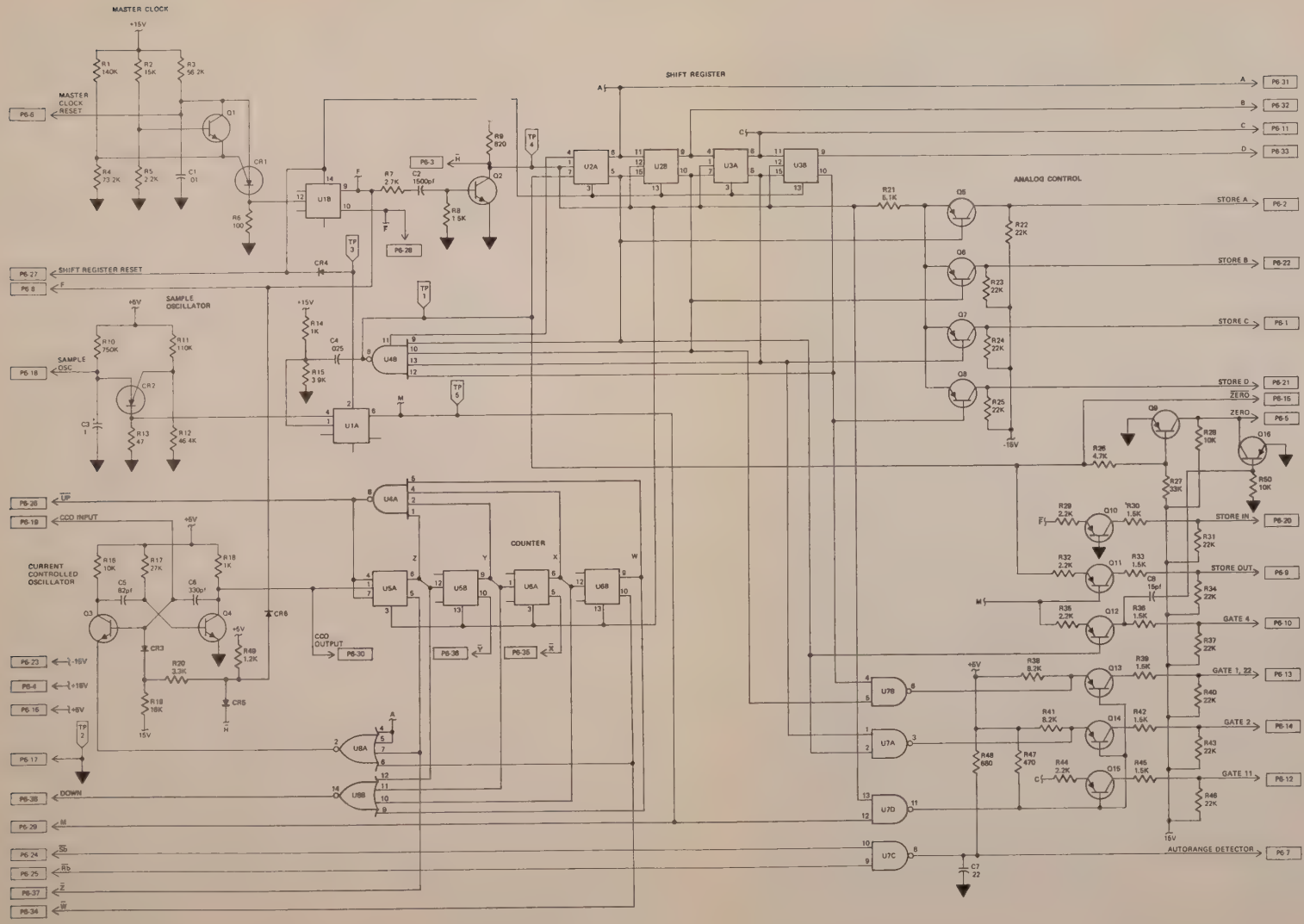
P.O. Box 7428 Seattle, Washington 98133

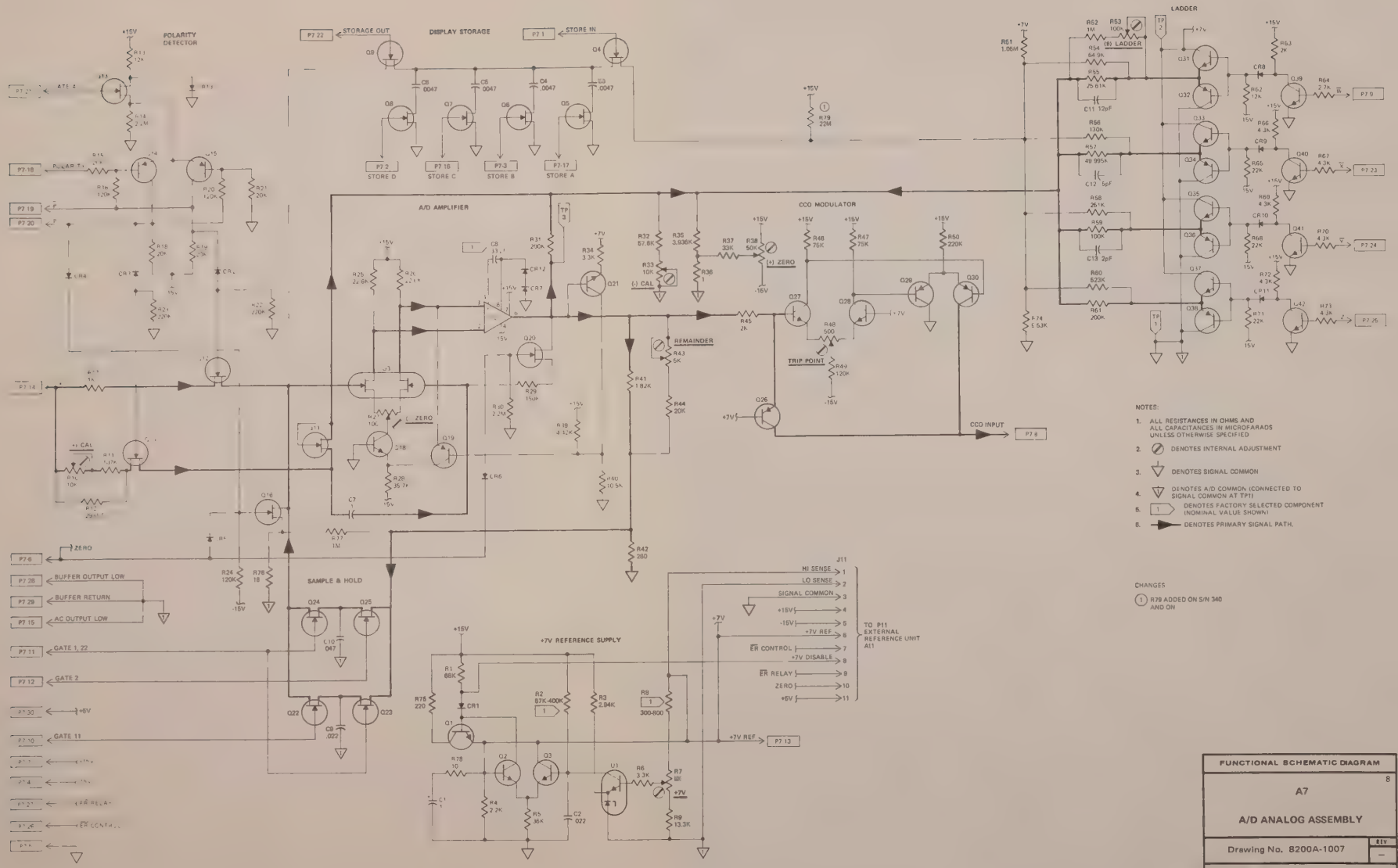


NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ▼ DENOTES LOGIC COMMON

IC	PIN CONNECTIONS	
	+5V	COMMON
U7, U4	14	7
U1, U2, U3, U5, U6	16	8
U8	8	1

FUNCTIONAL SCHEMATIC DIAGRAM	7
A6	
LOGIC CONTROL ASSEMBLY	
Drawing No. 8200A-1006	REV —
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT
3. ▽ DENOTES SIGNAL COMMON
4. ▽ DENOTES A/D COMMON (CONNECTED TO SIGNAL COMMON AT TP1)
5. ⬠ DENOTES FACTORY SELECTED COMPONENT (NOMINAL VALUE SHOWN)
6. ▬► DENOTES PRIMARY SIGNAL PATH.

CHANGES

(1) R79 ADDED ON S/N 340 AND ON

FUNCTIONAL SCHEMATIC DIAGRAM

8

A7

A/D ANALOG ASSEMBLY

Drawing No. 8200A-1007 REV —

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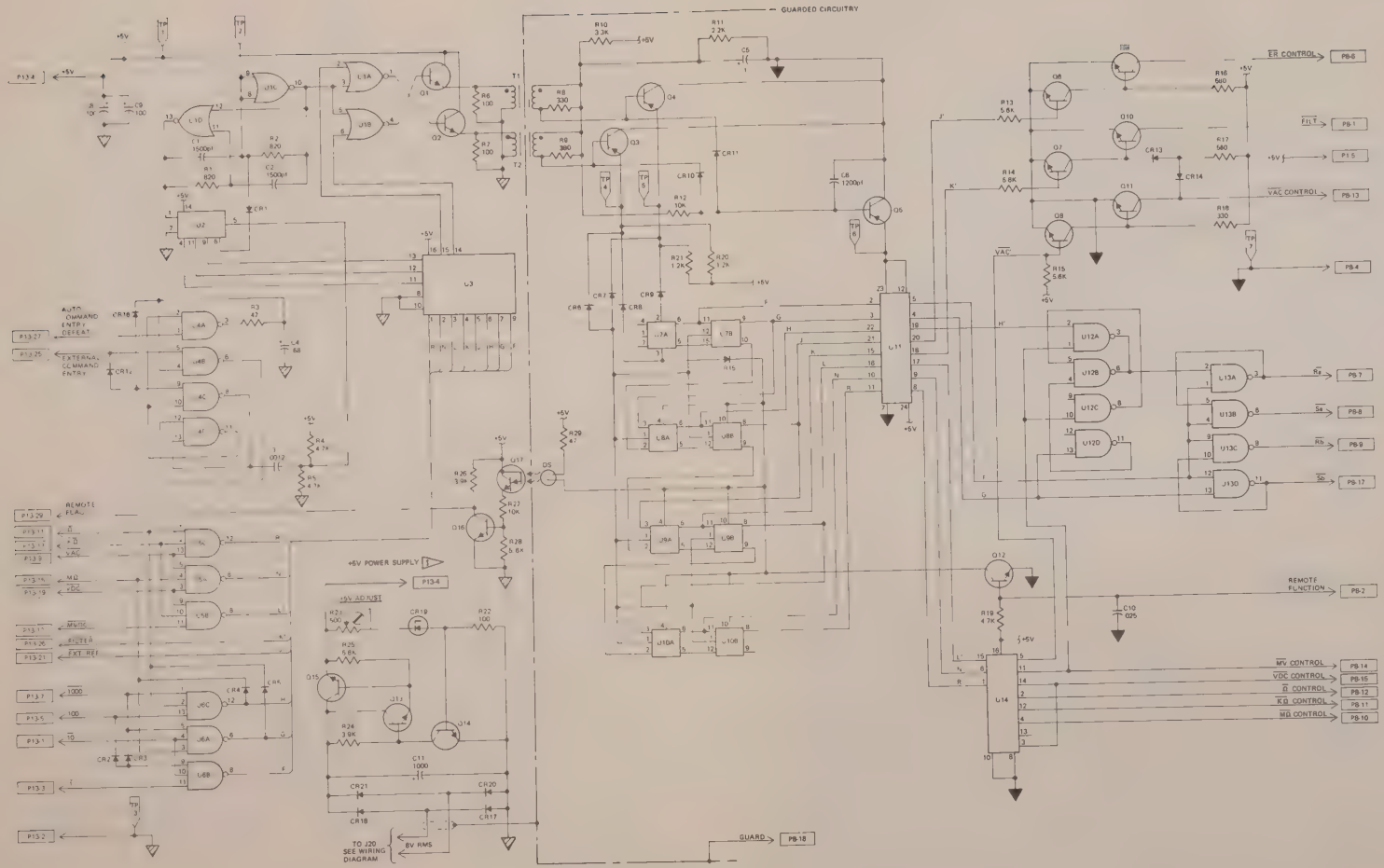


P13 TOP

P13 PIN CONNECTIONS AS VIEWED FROM REAR OF INSTRUMENT

BOTTOM

IC	PIN CONNECTIONS	
	+5V	COMMON
U1 U4 U6 U8-10 U12 U13	14	7
U3 U7	16	8

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⊘ DENOTES INTERNAL ADJUSTMENT.
3. ▼ DENOTES LOGIC COMMON.
4. ⏚ DENOTES EXTERNAL GROUND OR COMMON.
5. THIS POWER SUPPLY INSTALLED ONLY IN SPECIAL RCU, 8200A-05/AA. PROVIDES +5V LOGIC POWER TO RCU EXTERNAL GUARD CIRCUITRY IN LIEU OF DOU OR POU LOGIC SUPPLIES WHEN THESE OPTIONS ARE NOT INSTALLED. CONTACT FACTORY FOR DETAILS.

FUNCTIONAL SCHEMATIC DIAGRAM

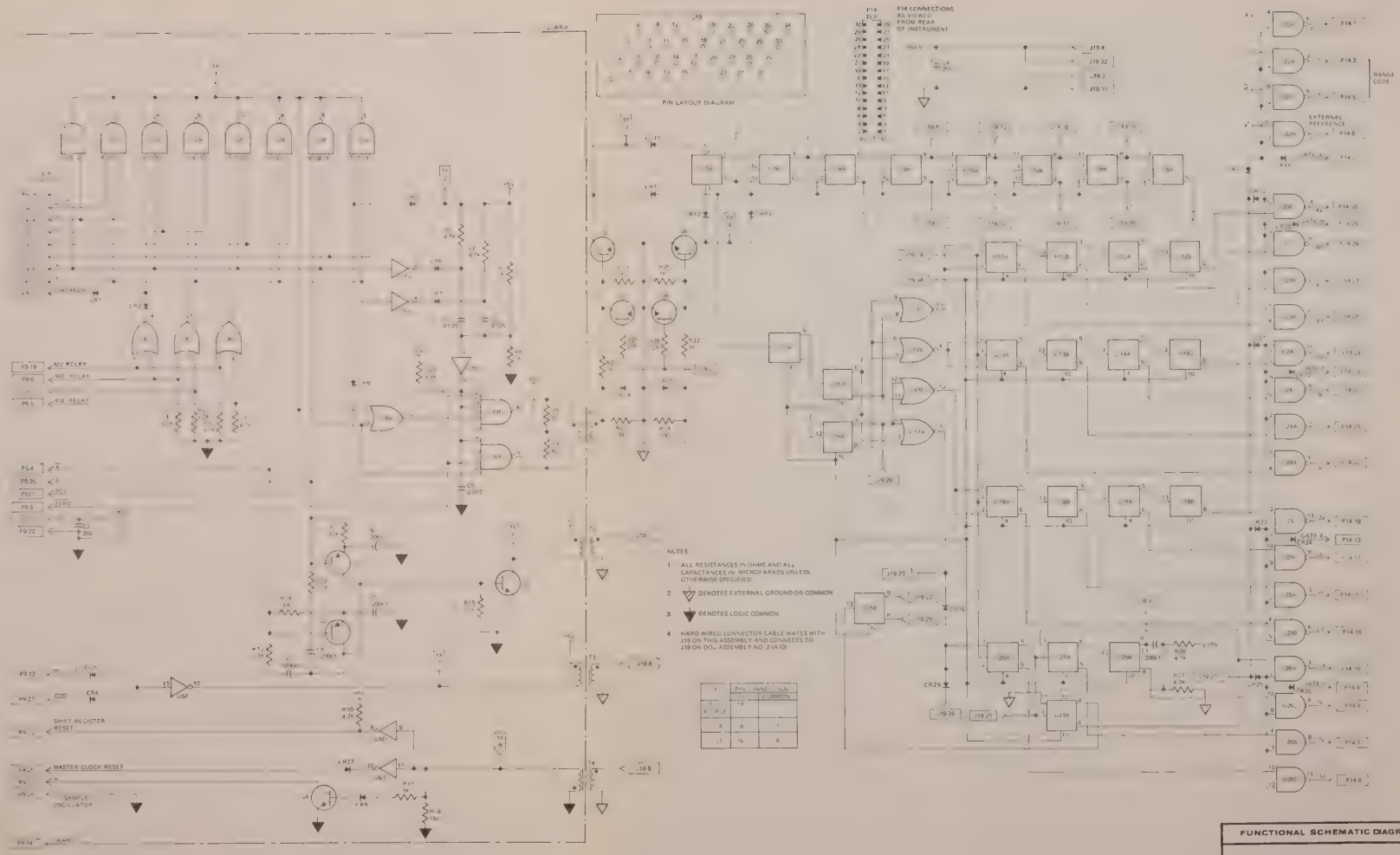
9

A8

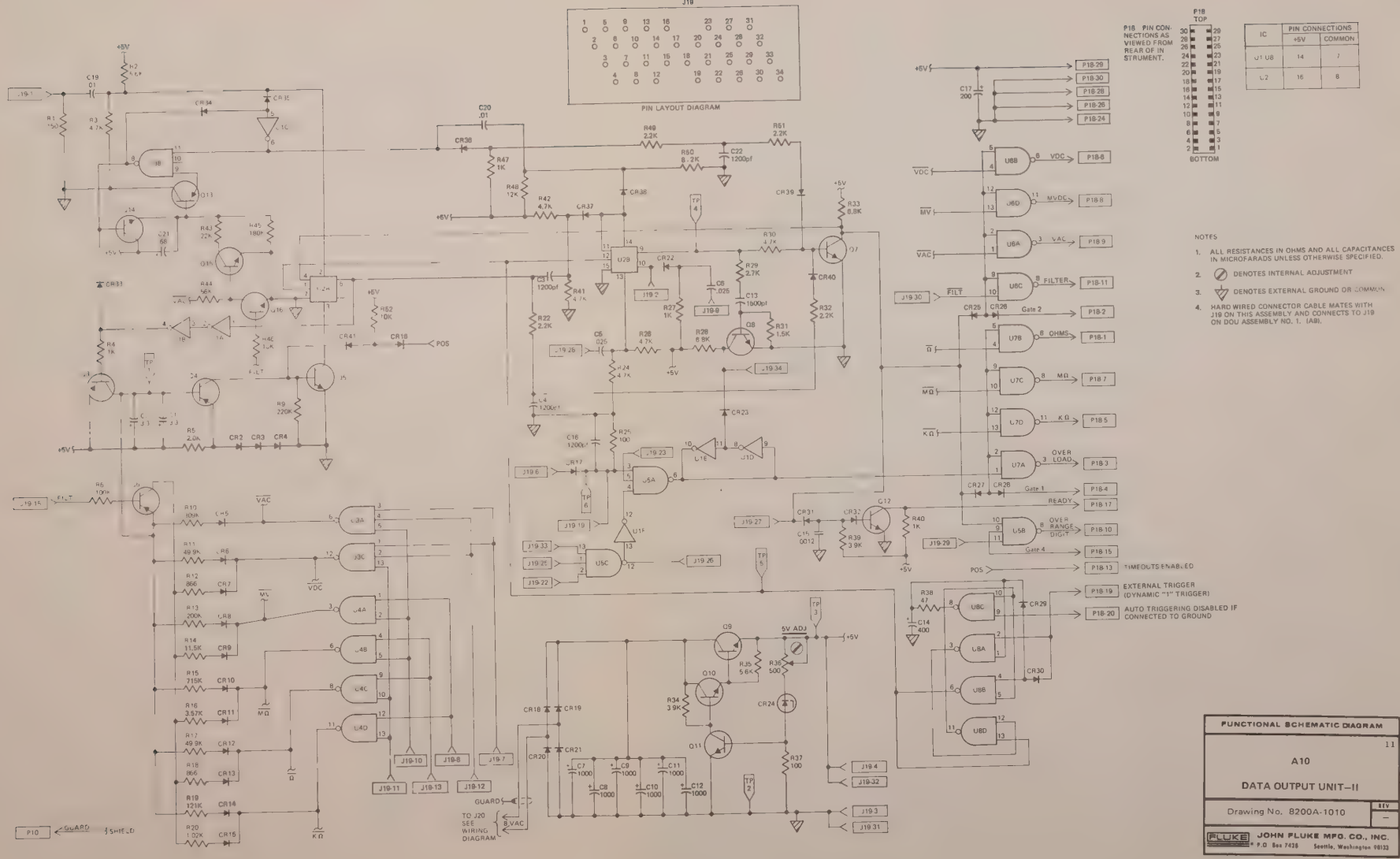
REMOTE CONTROL ASSEMBLY

Drawing No. 8200A-1008 REV —

FLUKE JOHN FLUKE MFG. CO., INC
P O Box 7428 Seattle Washington 98133



FUNCTIONAL SCHEMATIC DIAGRAM	
	10
A9	
DATA OUTPUT UNIT—I	
Drawing No. 8200A-1009	REV —
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



FUNCTIONAL SCHEMATIC DIAGRAM

11

A10

DATA OUTPUT UNIT–II

Drawing No. 8200A-1010

REV –

FLUKE JOHN FLUKE MFG. CO., INC.
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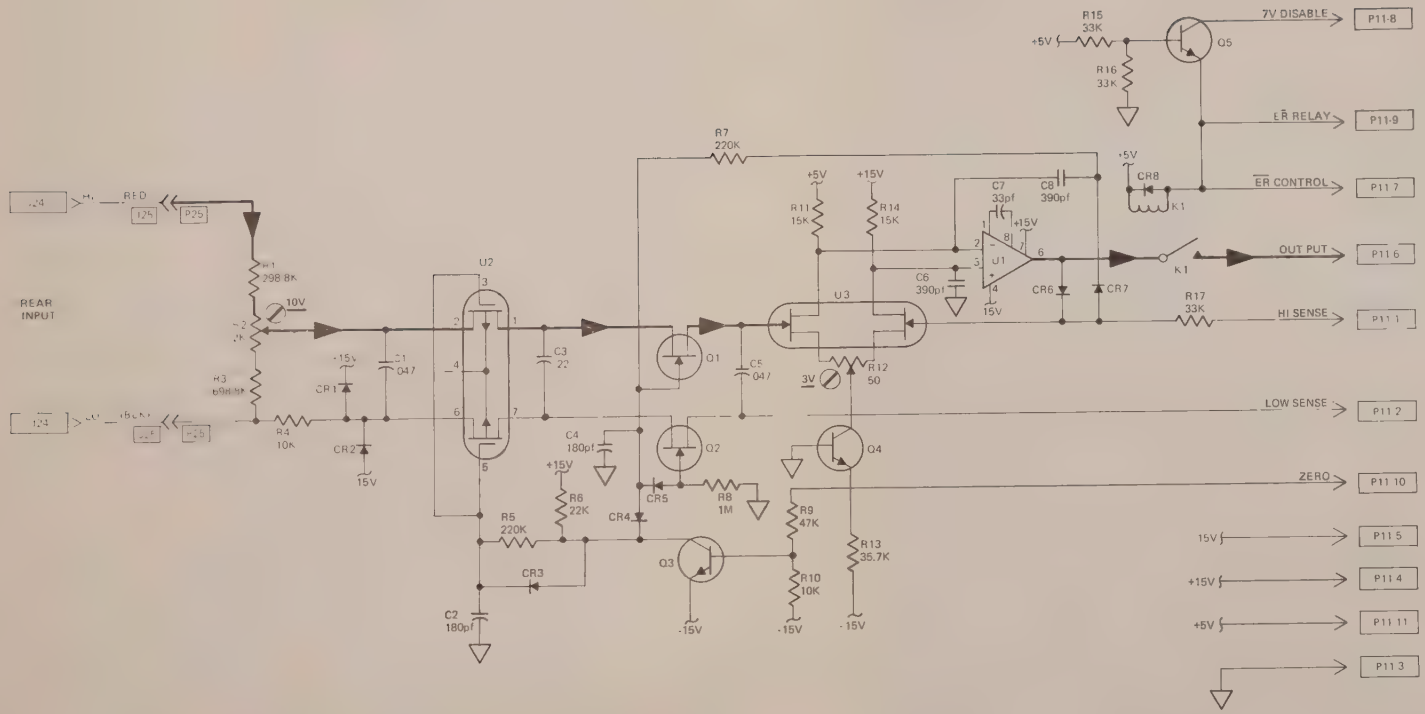

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. DENOTES INTERNAL ADJUSTMENT
3. DENOTES SIGNAL COMMON.
4. DENOTES PRIMARY SIGNAL PATH

FUNCTIONAL SCHEMATIC DIAGRAM

12

A11

EXTERNAL REFERENCE ASSEMBLY

Drawing No. 8200A-1011 REV —

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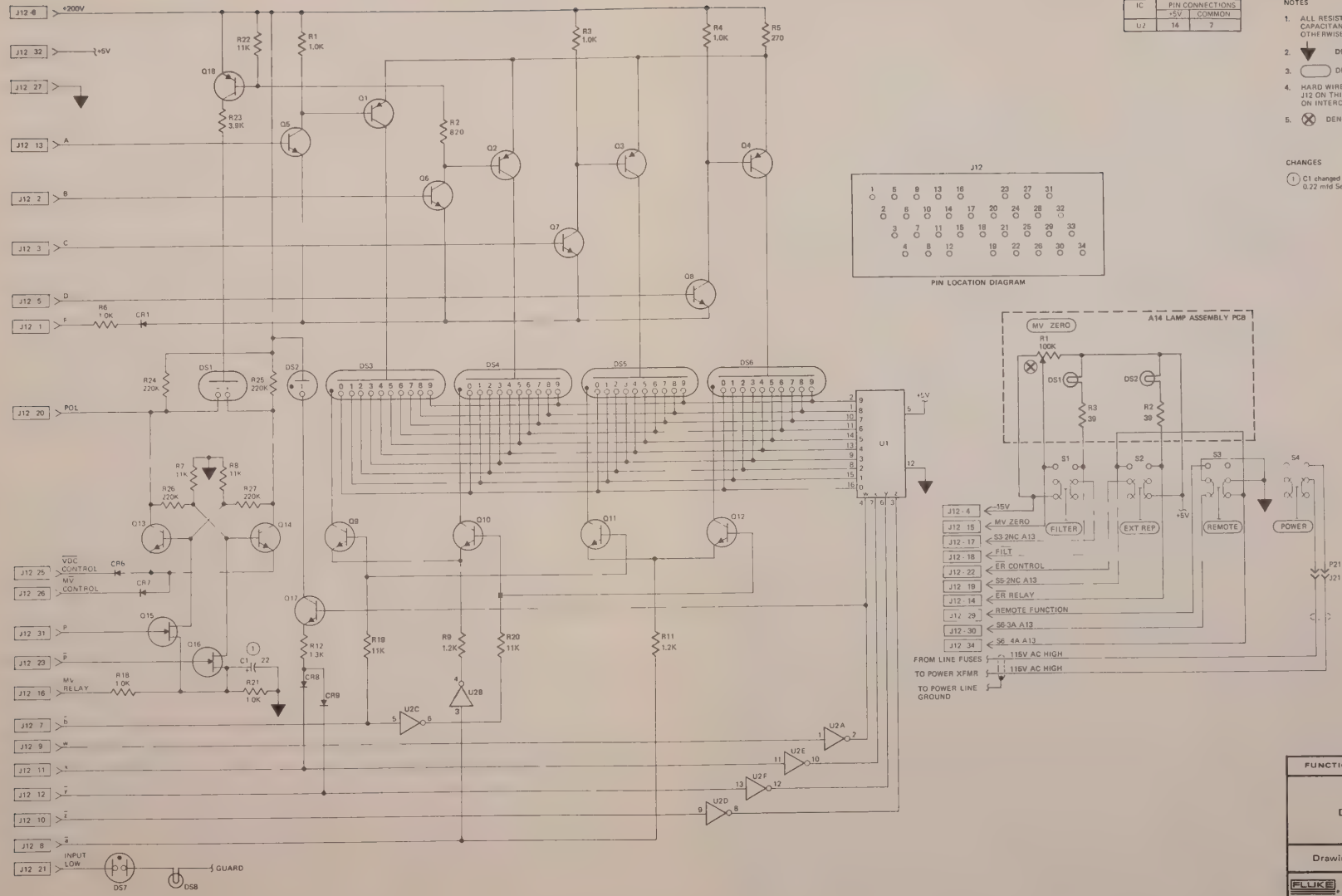

IC	PIN CONNECTIONS	
	+5V	COMMON
U2	14	7

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ▼ DENOTES LOGIC COMMON.
3. ▭ DENOTES FRONT PANEL LOCATION.
4. HARD WIRED CONNECTOR CABLE MATES WITH J12 ON THIS ASSEMBLY AND CONNECTS TO J12 ON INTERCONNECT ASSEMBLY A13.
5. ⊗ DENOTES FRONT PANEL ADJUSTMENT.

CHANGES

(1) C1 changed from 0.05 mfd to 0.22 mfd Ser No 249 and on

PIN LOCATION DIAGRAM

FUNCTIONAL SCHEMATIC DIAGRAM

13

A12

DISPLAY ASSEMBLY

Drawing No. 8200A-1012 REV —

FLUKE JOHN FLUKE MFG. CO., INC.
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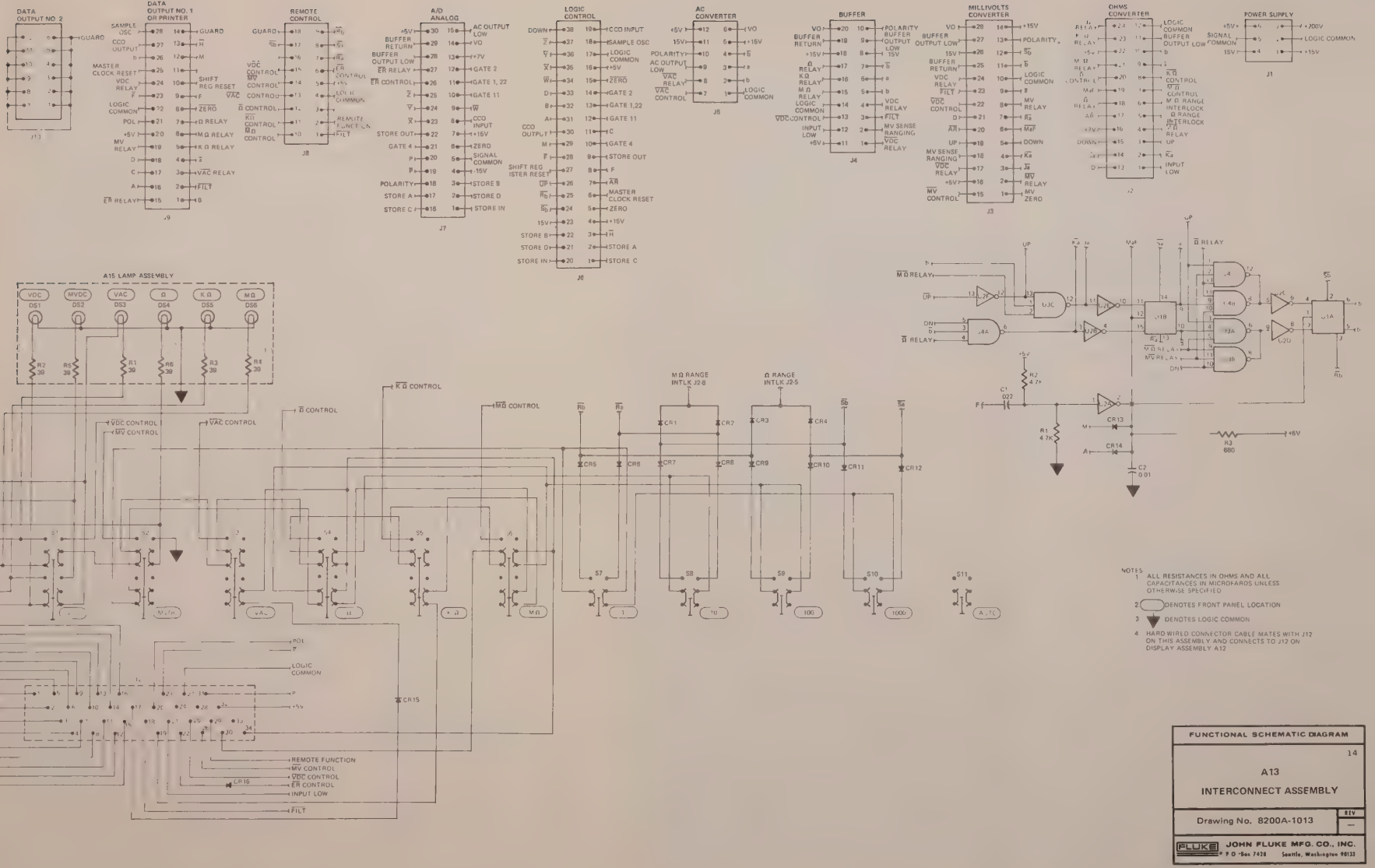

FUNCTIONAL SCHEMATIC DIAGRAM

14

A13

INTERCONNECT ASSEMBLY

Drawing No. 8200A-1013 REV —

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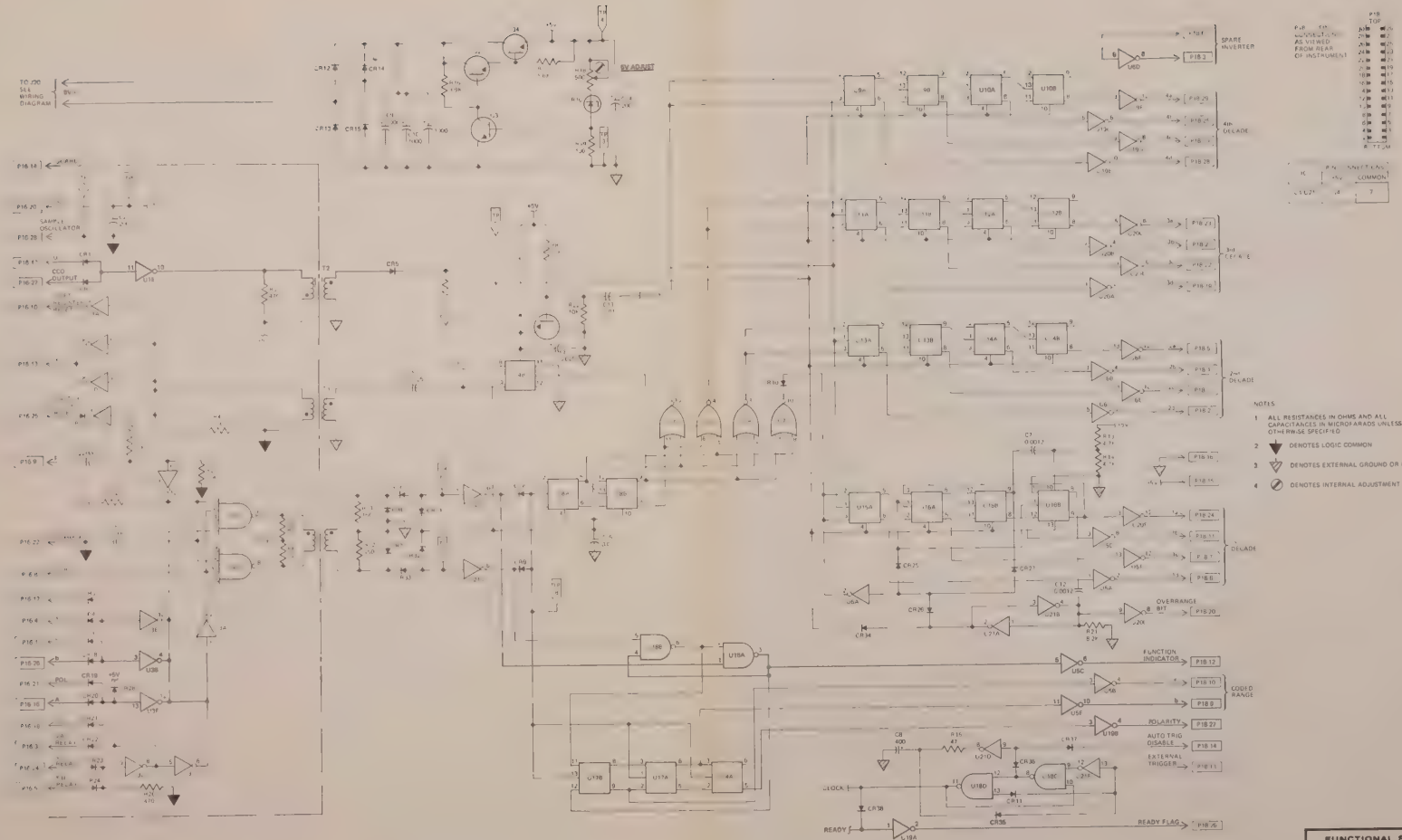
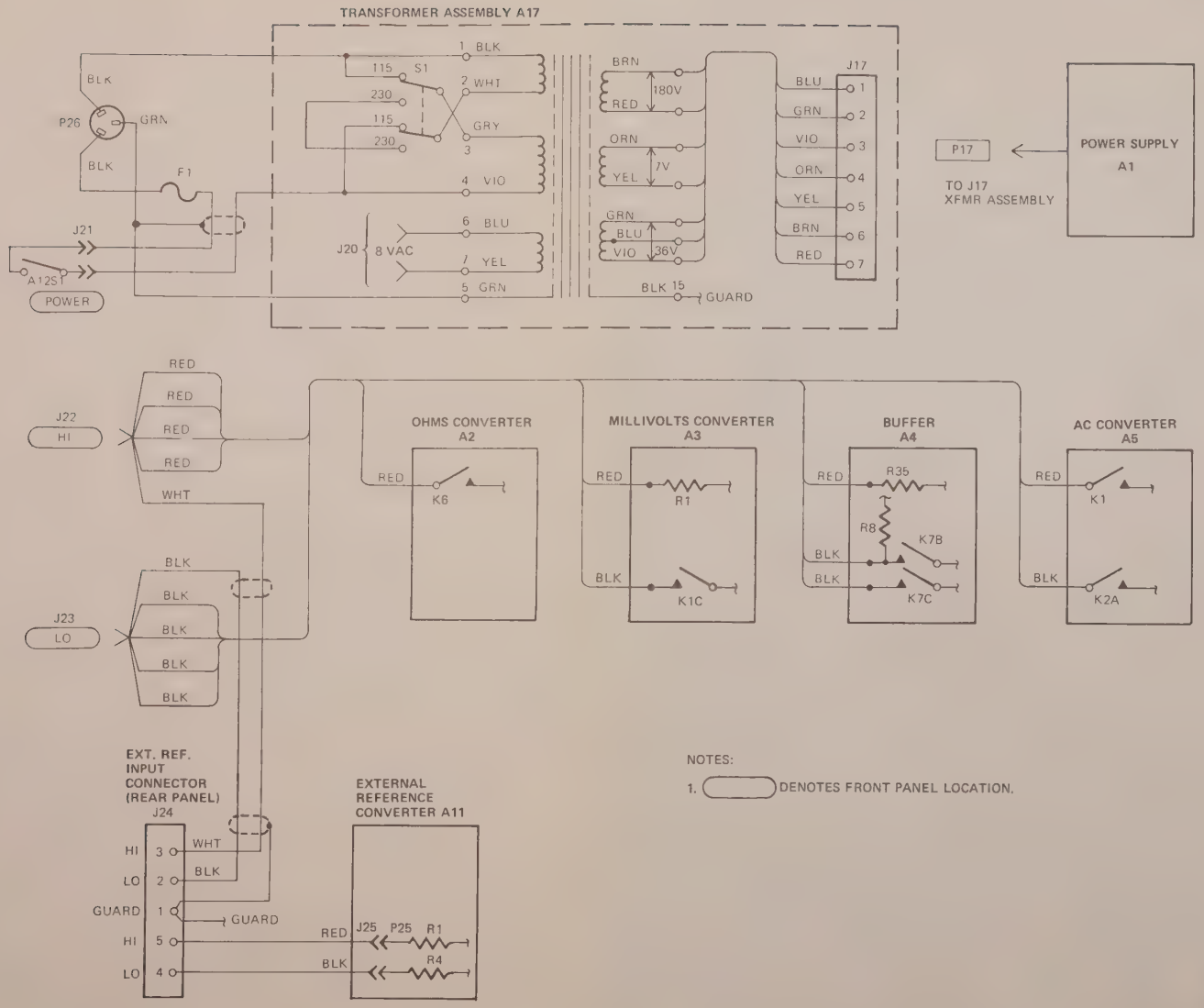


FUNCTIONAL SCHEMATIC DIAGRAM	
	15
A16	
PRINTER OUTPUT UNIT	
Drawing No. 8200A-1016	REV —
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



NOTES:

1. ( ) DENOTES FRONT PANEL LOCATION.

FUNCTIONAL SCHEMATIC DIAGRAM	16
WIRING DIAGRAM AND INPUT POWER SCHEMATIC	
Drawing No. 8200A-1000	REV –
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

II. BLOCK FUNCTIONS: (Figure 1)

A. Power Supply

The Power supply furnishes five voltages used in the instrument. +18, −18 operating supplies, +190 volt readout tube supply, +5 volt logic supply and +7 volt reference supply. Provisions are made for auxiliary supply of 5 volts required in the Data Output Unit option.

B. Buffer

The Buffer board assembly includes Function switching components. It has an input impedance that is greater than 10^{12} with an insertion current less than 50 pa. The Input Attenuator offers three ratios of voltage division 1/1, 1/10 and 1/100. Input limiting is provided to prevent damage to the instrument in any range with up to 1100 volts applied.

The total gain of the Buffer is 1 inverted with a low impedance output. Input filtering is included in this assembly which consists of a 60 Hz notch filter and a 3 pole low pass (30 Hz) filter. All frequencies above 50 Hz are attenuated by more than 60 db.

C. A-D Converter

Inverting Amplifier is used only when the input voltage being measured is negative. When the input to the instrument is positive, FET switches cause the output of the Buffer to bypass the Inverting Amplifier.

Polarity Detector circuitry automatically detects the polarity of the input signal and provides outputs for the logic switching of the Inverting Amplifier.

A-D Amplifier has two fixed gains and is one of the key elements in the Recirculating Remainder system of analog digital conversion system.

Ladders and Switches provide a voltage back to the summing junction of the A-D Amplifier and also a discrete voltage that is stored in the Analog Storage for use when the instrument is in the Storage Mode of operation.

Sample and Hold circuitry provides storage for the remainder voltages while the instrument is in the Measurement Mode of operation.

Analog Comparitor provides current to the Current Controlled Oscillator whenever the output of the A-D Amplifier exceeds the reference voltage of 7 volts.

D. Logic Section

A clock which operates at a frequency of 666 Hz produces a pulse train of 1.5 ms pulses, providing the timing for the entire instrument.

A 6 State Register divides the Clock pulses into six discrete time periods, which correspond to the ZERO time and the five digit times used in the instrument

Current Controlled Oscillator provides a pulse train whose output pulses are proportional in repetition rate to the current being supplied it. The pulses supplied by this oscillator are fed to the 16 State Binary Counter for decoding.

16 State Binary Counter receives the pulses from the Current Controlled Oscillator and converts them to Binary Coded Decimal (BCD) output in the standard 1-2-4-4 output.

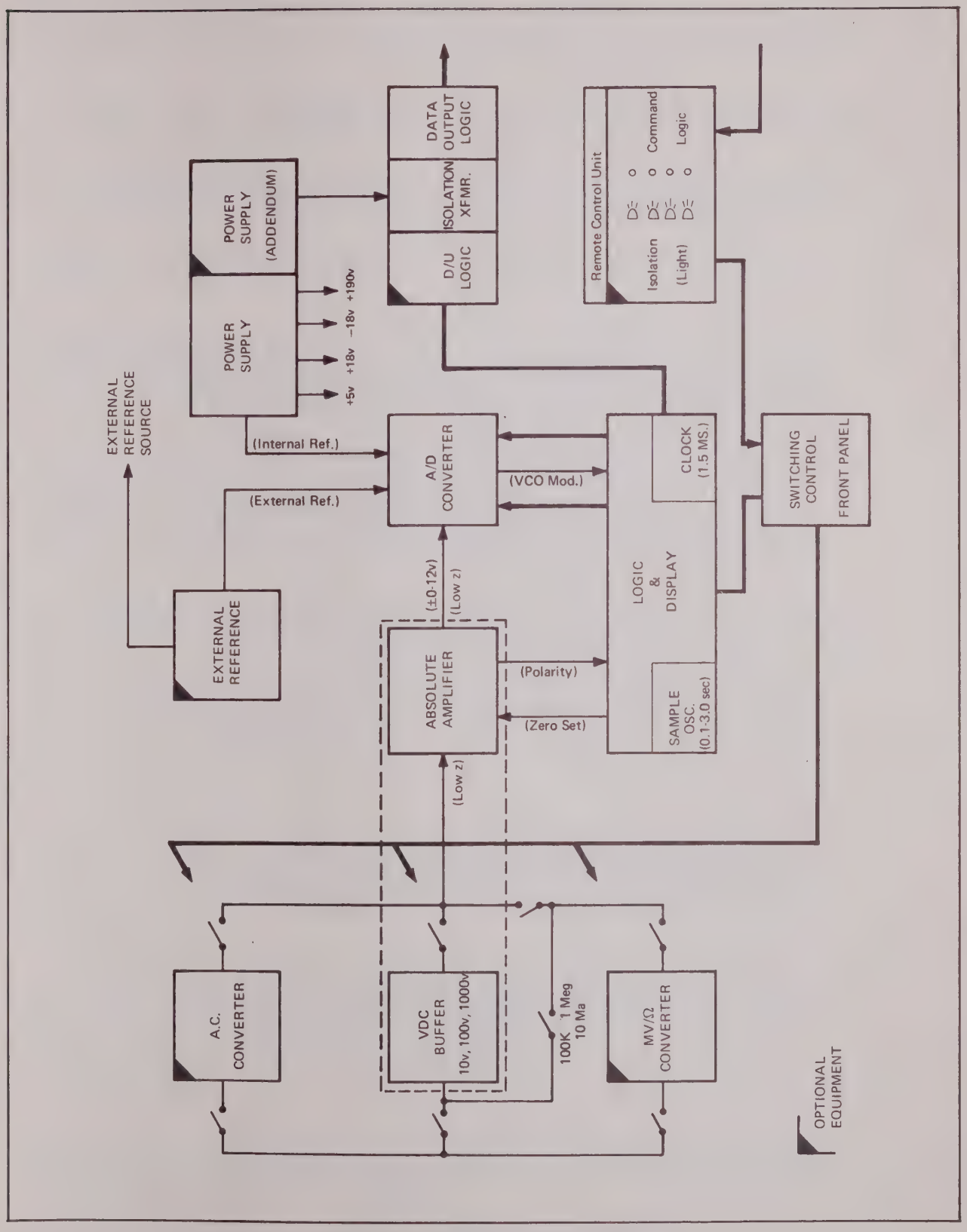


FIGURE 1. BASIC BLOCK DIAGRAM

Manual Range Controls are interlocked mechanically and electrically so as to provide priority to manual selections of function and range, preventing erroneous dial function or range commands.

Auto Range Controls are provided to accomplish automatic selection of the proper range via reed relays and functional logic packs.

Sample Oscillator provides a variable sample rate from once every 3 seconds to once every 100 milliseconds. Provisions for external sample rates up to 25 milliseconds are included.

Logic Section provides the solid state switching commands for both range and function controls.

E. Display

Anode Strobing circuit pulses each readout tube on for 1.5 ms during the appropriate time period of each complete cycle of the instrument. This means that during every 18 millisecond recycle period of the instrument each readout tube is only on for 1.5 milliseconds.

The BCD output of the 16 State Binary Counter is fed to the Decoder Driver where it is translated into decimal output. If the BCD code was 5 the Decoder Driver will apply ground to the five line to all readout tubes. Q31 through Q35 are enabled by the time period pulses A, B, C, D, E and the F pulse applied to the common emitters thus allowing the +190V to be applied to the proper readout tube for displaying the digits in sequence.

F. AC Converter

The input impedance is 1 megohm into the inverting amplifier. The gain is controlled by feedback switching. Rectification is accomplished by dual section half wave diodes.

Filtering is accomplished by a 3 section RC filter combined with large feedback loop capacitors. The output of the filter is fed to a times 10 Inverting Amplifier which feeds the A-D Converter of the instrument.

G. Millivolt/Ohms Converter

In millivolt operation a chopper stabilizer operational amplifier is used which feeds an intergrated circuit operational amplifier with a gain of 10 on the 1000 millivolt scale and a gain of 100 on the 100 millivolt scale. The output of the millivolt section of the converter is 0 to 12 volts DC.

In Ohms operation the converter uses the +7 volt reference to supply current to the unknown resistance and the voltage drop across the resistor is translated by the instrument into ohms values. The instrument input is so configured as to provide modified four terminal resistance measurements for additional accuracy.

H. External Reference

This option provides a means of referencing the instrument to external sources from 2 to 10.5 volts via a chopper stabilized operational amplifier to increase the isolation between the system under measurement and the 8300.

III. SUB-SECTION FUNCTIONS

A. Power Supplies (Figure 2 and Schematic No. 5)

The primary windings are so configured as to provide either 115 VAC or 230 VAC input power which is selected by a switch on the rear panel.

The +18 volt supply is zener regulated and provides the initial reference for the other supplies, so if trouble exists in the +18 supply it is reasonable to expect that all of the other supplies will also show a problem.

The −18 volt supply is referenced to the +18 volt supply by the voltage drop across R231, R223.

The +5 volt supply, which is used for the logic functions is regulated by the voltage drop appearing across the +18 volt supply and R229.

The +7 volt reference supply is regulated by zener pack A201. The voltage to this circuit is fed by the +18 volt supply.

The +190 volt supply for the readout tubes is regulated by a voltage division which is referenced to the +18 volt supply.

B. Buffer (Figures 3, 4, 5, 6 and Schematic No. 1)

The buffer pre-amplifier of the 8300A is basically an inverting unity gain voltage follower. Its primary function is to provide an impedance conversion between the signal source being measured and the A-D Converter input.

Referring to Figure 3, the buffer could be represented as shown. The input resistance of the buffer is $\frac{E_s}{I_s}$ If I_s can be kept small, then the impedance will be high. The resistance R_L is the leakage resistance between the High and Low input termianls. Care was taken in the mechanical design of the instrument so that the leakage resistance would always be greater than 10^{12} ohms.

The other component of I_s is I_e. Elementary feedback theory indicates that the input resistance of an amplifier connected as shown in Figure 3 will be the product of the open loop input resistance and the loop gain. Junction Field Effect J-FETs, are used in the inputs of the buffer, and thus an open loop input resistance of greater than 10^9 ohms is obtained. The loop gain of the buffer is approximately 10^6, so the input resistance of the actual amplifier is greater than 10^{15} ohms, or much greater than the leakage resistance than could be expected at the input terminals.

Using J-FETs also helps keep the insertion current of the buffer preamplifier less than 50 pa. That means that a source resistance of 1 megohm would cause less than 50 μV or ½ digit of offset due to injection current.

The A-D converter has a full scale input of 12 volts, thus requiring a means of reducing input signals greater than 12 volts, if they are to be measured. For that purpose, a 10 megohm attenuator can be placed in front of the buffer when the input exceeds 12V.

The attenuator has two ratios available. One provides a division of 10 and the other provides a ratio of 100. Both are controlled by the front panel switches or the Remote Control Unit. In the 1000 volt range, the divider ratio is 1/100 and in the 100 volt range the ratio is 1/10. In the 10 volt range the input is direct.

The attenuator connection is as shown in Figure 4, with range commands adjacent to each switch. Limiting circuits are provided at the amplifier input, in series with current limiting resistors so that ±1100 volt signals cannot damage the buffer, even in the 10 volt range.

A zeroing circuit (R47) is provided on the buffer for calibration. The excellent zero stability of the FET pair used at the buffer input makes it unnecessary to provide front panel adjustment.

In addition to providing impedance buffering and signal attenuation, the buffer pre-amplifier also can be called upon to filter the input signal. Internal to the amplifier are roll off networks

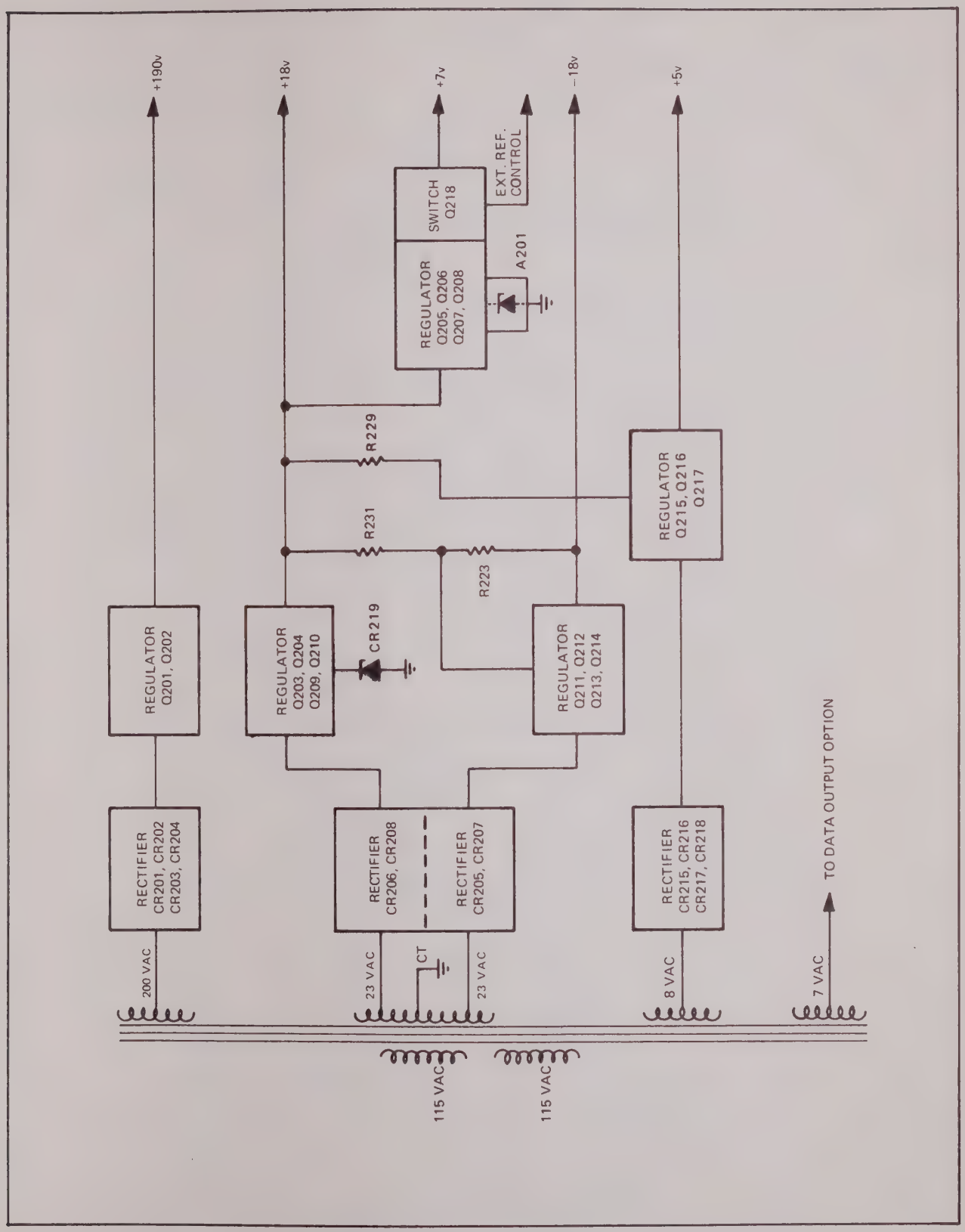


FIGURE 2. 8300A POWER SUPPLY

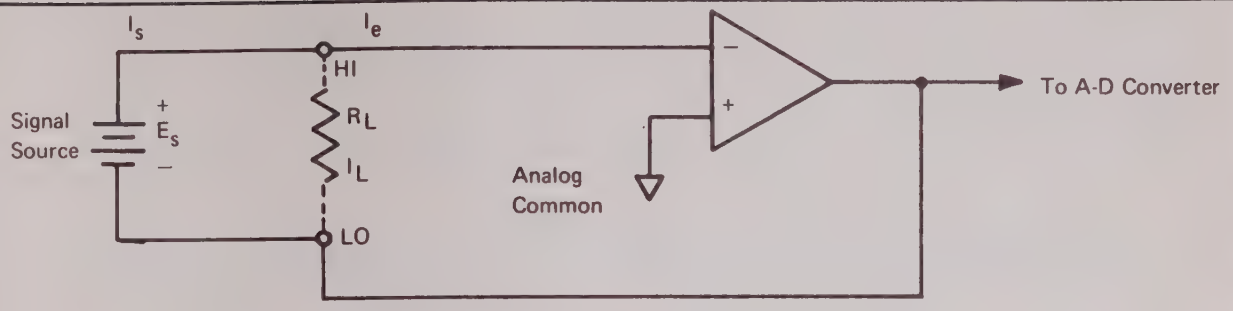


Figure 3. BUFFER

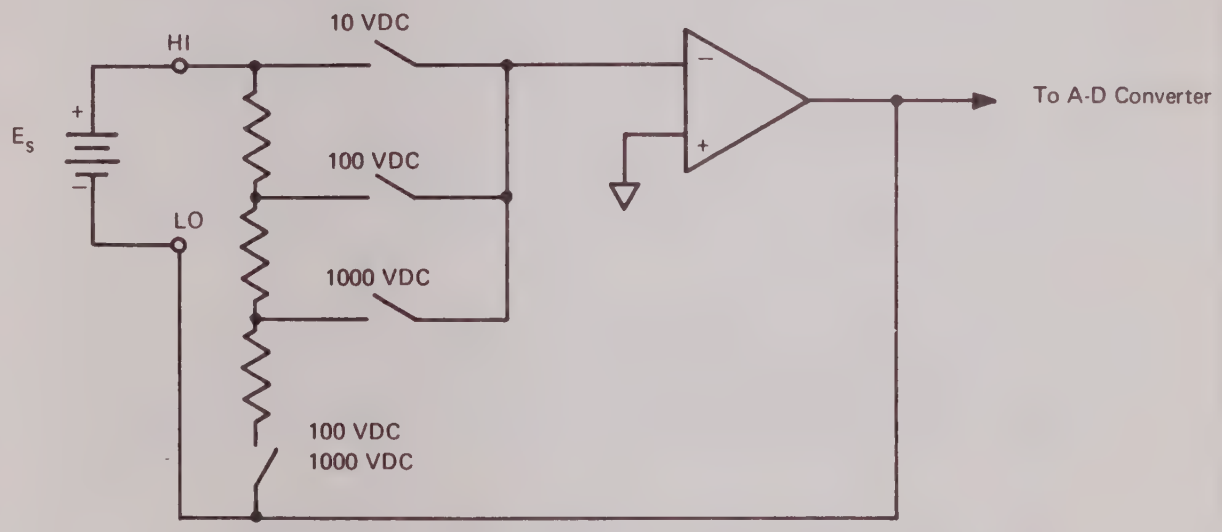


Figure 4. BUFFER WITH ATTENUATOR

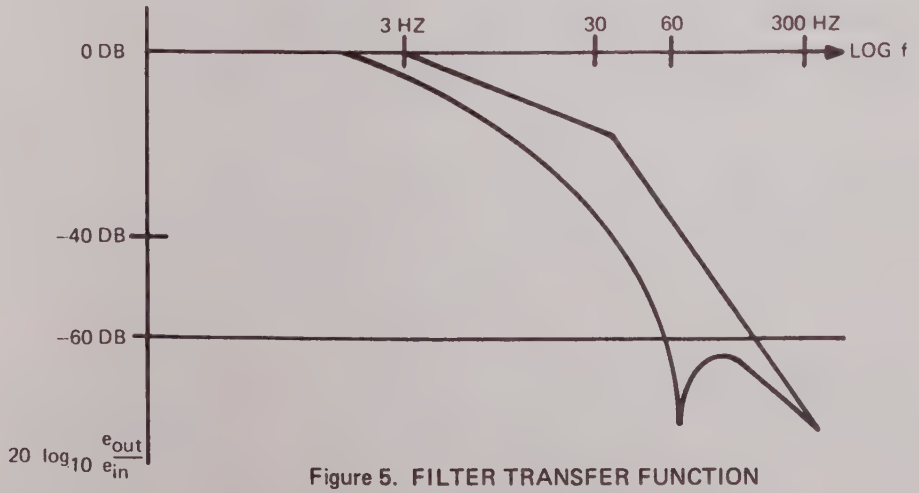


Figure 5. FILTER TRANSFER FUNCTION

that establish a unity gain frequency of 3 Hz. This roll off of the gain of the buffer provides high frequency filtering by attenuating the AC signals inside the buffer and presenting a reduced version of the AC signal input to the A-D Converter. The frequency characteristics are shown in Figure 5. A notch filter is provided at 60 Hz and three pole response is present above 30 Hz. As the figure shows, for all frequencies above 50 Hz, the rejection of AC signal at the input is greater than 60 db.

Up to now the buffer has been considered as a single block amplifier. A more detailed explanation of circuit operation is in order. The block diagram shown in Figure 6 is complete enough for signal tracing. For illustration, place a positive DC voltage across the HI and LO input terminals.

Since AMP 1 is a high gain operational amplifier with its inverting terminal grounded, any signal at the non-inverting terminal will produce a large in -phase version of that signal at the amplifiers output. AMP 2 is connected inside of its own feedback loop to give a negative gain of about 2.5. When the amplified positive signal at the output of AMP 1 is applied to AMP 2's loop, the result is that the output of AMP 2 is driven negative. The voltage to which the output of AMP 2 is driven is determined solely by the input signal applied and the voltage to which the non-inverting input of AMP 1 is driven. Since the loop gain of the buffer is very high, the positive input of AMP 1 effectively does not change, and as pointed out earlier, the FET input does not allow any current flow from the source. Because there is no voltage present with respect to the analog common at the positive input of AMP 1, and because no current can flow from the source, the output of AMP 2 can only go to $-E_s$ with respect to analog common. Thus, we have an inverting voltage follower.

When FILTER is called with the 8300, large capacitors are placed in the feedback paths of both AMP 1 and AMP 2. In addition, both a notch filter and a low pass filter are placed in the forward gain path. The feedback capacitors force the 3 Hz unity gain bandwidth for the buffer, the notch filter provides 60 Hz filtering, and the low pass filter adds two additional poles at effectively 30 Hz.

C. A/D Converter (Figures 7, 8, and Schematic No. 2)

Referring to Figure 7 the time relationships can more easily be visualized. The Master clock generates timing pulses, which are fed to the clock input of a J-K flip-flop, 3F, which produces the F and $\overline{F}$ pulses. The F pulse is further modified by Q1 where the $\overline{H}$ pulse is generated. The $\overline{H}$ pulses are fed to the clock inputs of the 6 State Shift Register, where five of the six timing pulses are generated. The sixth, $\overline{ZERO}$ pulse is generated by the action of the NAND gate 4B. Note that it is possible to divide any of the time periods into two equal parts by using the F and/or the $\overline{F}$ pulses. (These time periods are refered to as A1, A2, B1, B2 . . . etc.)

During the ZERO time period the $\overline{ZERO}$ pulse operates the A-D Auto Zero Drive Circuit. Q118 conducts and connects the output of A2 to the zero holding capacitor C115 and at the same time the input of the amplifier is grounded. This operation places the offset of A2 across C115 and effectively removes it for the remainder of the cycle. A similar circuit removes the offset from the Inverting Amplifier during "C" period of time.

For the purposes of illustration, it is necessary to make several assumptions and specify several conditions. The assumption is made that ranging functions are complete and that a voltage of –6.3524 volts is appearing at the input to the main chassis. (R102) The instrument is entering a Measurement Cycle.

The –6.3524 volts is amplified and inverted by the Inverting Amplifier and appears at the Polarity Detector which is enabled by Gate 4 pulse. The voltage is now positive due to the action

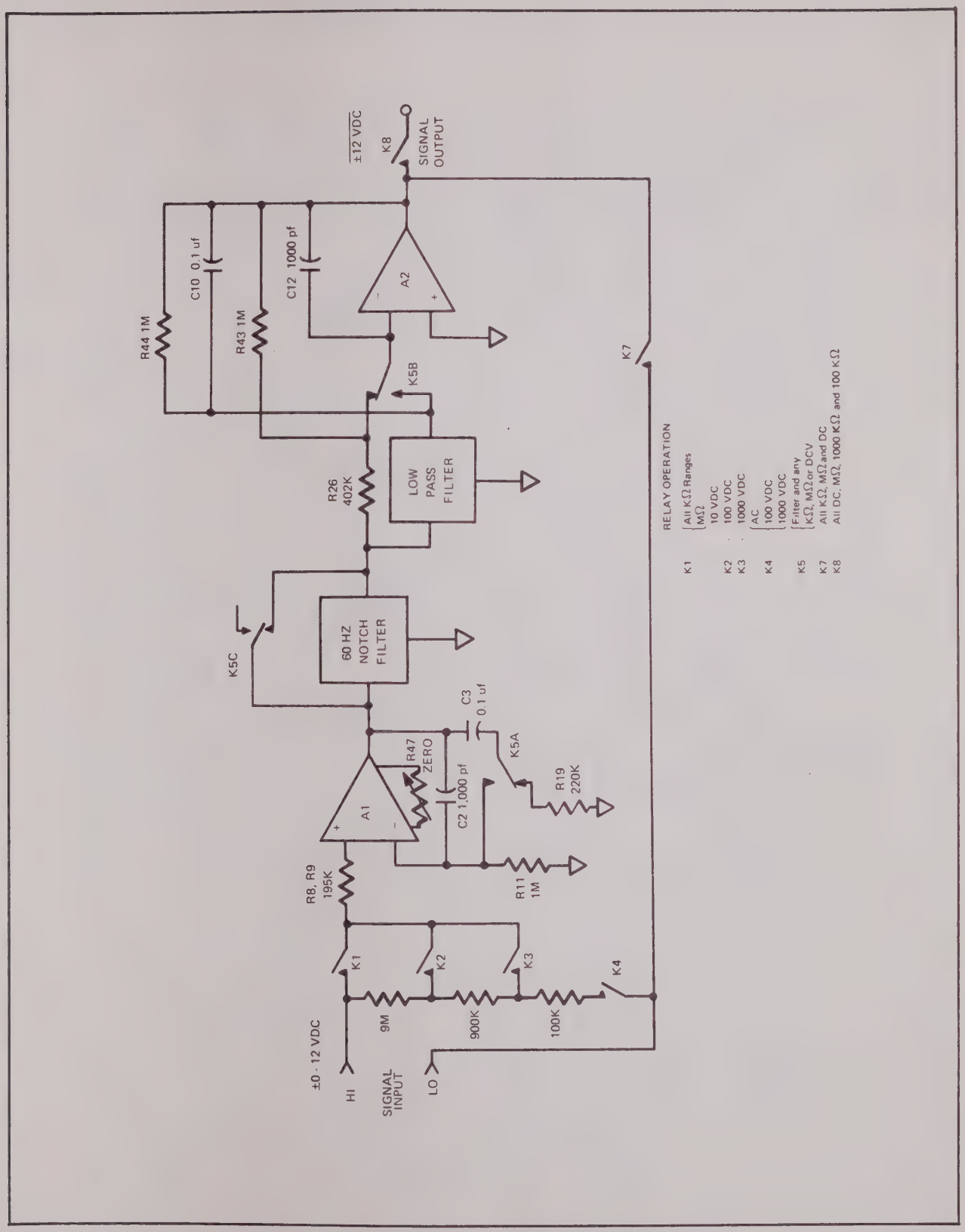


FIGURE 6. BLOCK DIAGRAM OF BUFFER

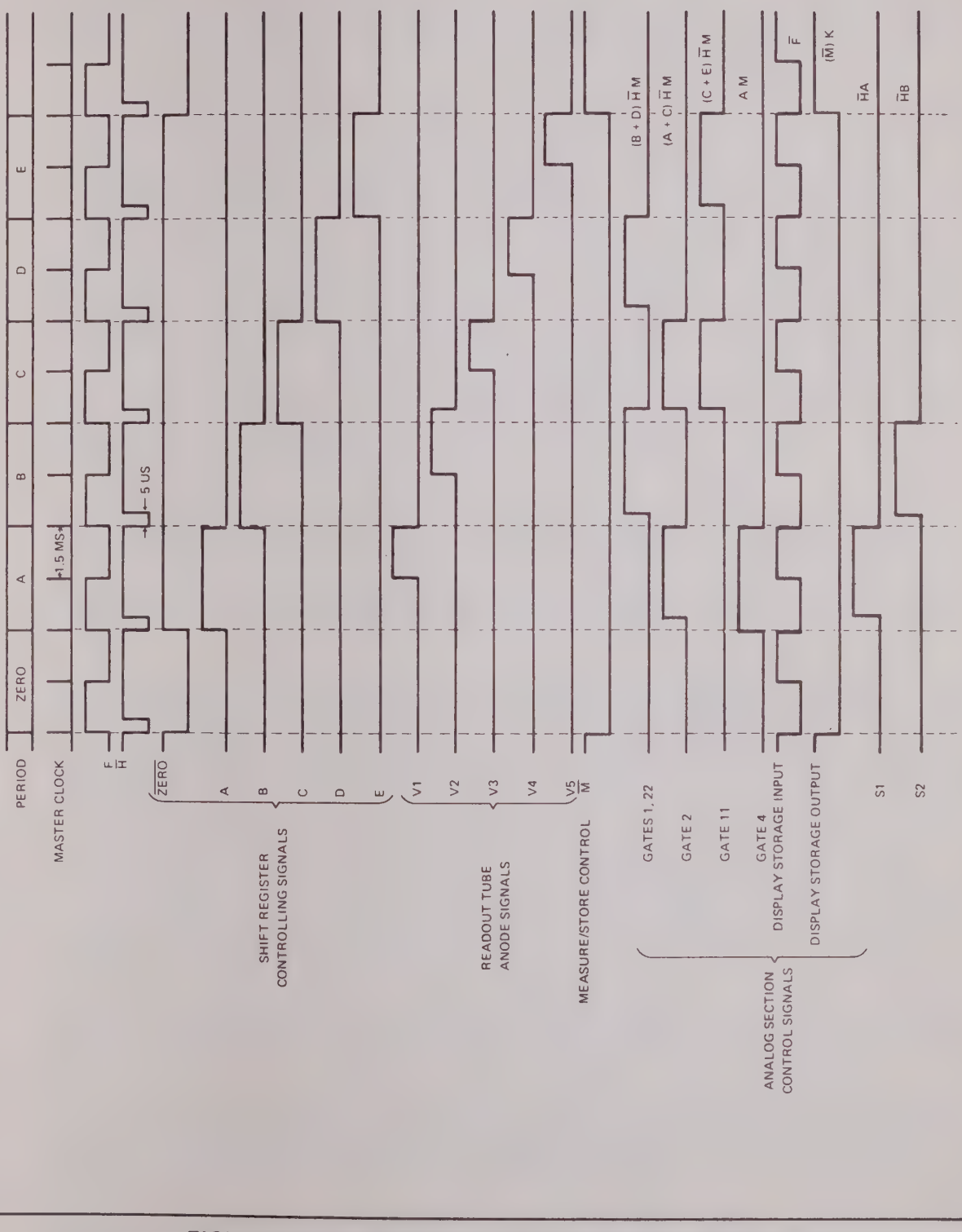


FIGURE 7. MEASUREMENT CYCLE TIME RELATIONS

of the Inverting Amplifier. The positive output to the Polarity Detector will cause the Polarity Detector to turn the plus gate Q112 on. This will cause the negative input to R102 to move directly to the input of the A-D Amplifier through R166. (In the case just taken the input to the instrument would have been positive. Had the input been negative, the Polarity Detector would have turned on the Minus gate, Q111 and the incoming signal would have been inverted by the Inverting Amplifier. This output is fed to the A-D Amplifier through R165.

NOTE: The inverting amplifier is used only when the input to the 8300A is negative.

The negative voltage appearing at the inverting input to the A-D Amplifier will cause a positive voltage to appear at its output. When the output of the A-D Amplifier exceed the 7.0 volt reference, the Analog Comparitor will produce current. This current is fed to the Current Controlled Oscillator (CCO). The Current Controlled Oscillator will produce a pulse train whose repitition rate is proportional to the current being supplied. These pulses are fed to the 16 State Binary Counter where they are translated into Binary Coded Decimal (BCD) output. The BCD output is connected to the Ladder Driver circuits and with each incremental increase of digit value the ladders will produce a current step. When the Primary Ladder has been caused to step 6 times the output from the Ladder being fed back to the input of the A-D Amplifier will cause the amplifier to satisfy itself with an output of less than 7 volts. At this time the Analog Comparitor will no longer supply current to the Current Controlled Oscillator and no further pulses will be generated. The remainder voltage that appeared at the output of the A-D Amplifier to satisfy it is now applied to capacitor C118 through Q125 which was enabled by the Gate 2 pulse (Sample and Hold)

The secondary Ladder output is fed to capacitor C110 in Display Storage. The BCD output of the 16 State Binary Counter is also fed to the Decoder Driver, where it is decimalized, which will cause ground potential to appear on the "6" line to all readout tubes. The A pulse and the F pulse are fed into the Anode Strobing Control which will cause the +190 volts to be pulsed on during the last half of the A time period, thus causing the "6" to be displayed by the first readout tube.

At the beginning of the B time period the $\overline{H}$ pulse will reset the 16 State Binary Counter. The Gate 1 & 22 pulse will enable Sample and Hold transistors Q124 and Q127. The remainder voltage stored on capacitor C108 is now applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and again the Analog Comparitor will produce current, which is fed to the Current Controlled Oscillator. The oscillator pulses are counted by the 16 State Binary Counter and converted to BCD. The Ladders are caused to increase their output incrimentally with each pulse until the Primary Ladder feeds a "3" pulse back to the summing junction of the A-D Amplifier. At this time the output of the amplifier is less than 7 volts which causes the Analog Comparitor to stop the current flow to the Current Controlled Oscillator. Etc. The remainder voltage appearing at the output of the A-D Amplifier is applied to capacitor C109 in the Sample and Hold circuit through Q127. The Secondary Ladder output is stored on Display Storage capacitor C111 through Q129 and Q147.

Again the Decoder Driver has caused a ground potential to appear on all of the "3" lines to the Readout tubes and the F pulse through CR105 and the B pulse through Q34 will cause the +190 volts to be applied to the second readout tube, where the digit "3" will be displayed.

The process continues using alternately capacitors C108 and C109 in the Sample and Hold circuit to store the remainders and then reapply them to the summing junction of the A-D Amplifier. As each time period digit is developed, the Secondary Ladder stores its output on seccessive capacitors in the Display Storage capacitors C110 through C114.

It is well to remember that the above description was of a Measure Cycle. All of the digits were developed using the Sample and Hold circuit. The following description is of the Storage Cycle.

Gate pulse 4 is the primary control over the determination of whether the 8300A will enter a Measure Cycle or a Storage Cycle. If Gate 4 pulse is not present the Polarity Detector will not be activated and the instrument will continue in Storage Cycle. Gate 4 pulse is generated by Q116 and will only be present in A period when an M signal is present.

Since in this example we are entering a Storage cycle no Gate 4 signal will be present and Q146 in the Display storage will be enabled. The last Measurement Cycle left incremental voltages stored in the Display Storage capacitors C110 through C114 that correspond to the digits 63524.

During the A period Q128 and Q146 will be enabled allowing the voltage stored in C110 to be applied to the input to the A-D Amplifier. The output of the amplifier will exceed 7 volts and the Analog Comparitor will supply current to the Current Controlled Oscillator. The oscillator will generate a series of pulses causing the 16 State Binary Counter to translate the pulses into BCD output. The BCD output will cause the Ladders to switch until the Primary Ladder output satisfies the A-D Amplifier feedback. At this point in time the output from the amplifier will be below 7 volts and the Analog Comparitor will no longer supply current to the CCO. The pulses stop and the output of the Secondary Ladder will again be stored in capacitor C110 in the Display Storage circuit. The BCD 6 from the 1 6 State Binary Counter will drive the Decoder Driver which will produce a ground potential on all of the "6" leads to the readout tubes. The combination of A and F pulses will cause Q35 and Q40 to apply +190 volts to the anode of V1 which will light the "6".

During the B period, Q129 and Q147 will be enabled, applying the voltage stored in C111 to be applied to the summing junction of the A-D Amplifier. The output of the A-D Amplifier will exceed the 7.0 volt reference and the analog comparitor will supply current to the Current Controlled Oscillator. The pulses from the CCO will be counted and translated to BCD output by the 16 State Binary Counter.

The BCD output being applied to the Ladder Driver Circuits will cause the ladders to increase their outputs until the output of the Primary Ladder, which is fed back to the summing junction of the A-D Amplifier satisfies the amplifier. At this point in time the output of the amplifier will be below the 7.0 volt reference and the Analog Comparitor will no longer furnish current to the CCO and the pulses will stop. Since a "3" was digitized and stored in the Display Storage for this time period, a three from the Primary Ladder will cause the A-D Amplifier to be satisfied. The output of the Secondary Ladder will be stored in the Display Storage during the last half of the time period and the "3" will be displayed by V2 during the last half of the time period by the operation of the Anode Strobing Control.

Each increment of voltage stored in the Display Storage will be digitized and re-stored in the Display Storage circuit until all five digits have been displayed. At the end of the Storage Cycle if no Measure pulse has been generated prior to A time the 8300A will again enter a Storage Cycle. This process will repeat until a Measure pulse is generated, prior to A time and then at A time a Gate 4 pulse will be generated and the instrument will again sample the input voltage and enter a Measurement Cycle.

Refer to Figure 8 for a recap of the Measurement Mode and Storage Mode of operations.

D. **Logic Section (Figures 7, 9, 10, 11, 12 and Schematic No. 3 sheets 1 and 2)**
The Master Clock provides the timing for the entire instrument. The pulses from the flip-flop are fed to the clock input of a J-K flip-flop where the F and $\overline{F}$ pulses are generated.

The F pulse is then applied to Q1 where the $\overline{H}$ pulse is generated. (Figure 7).

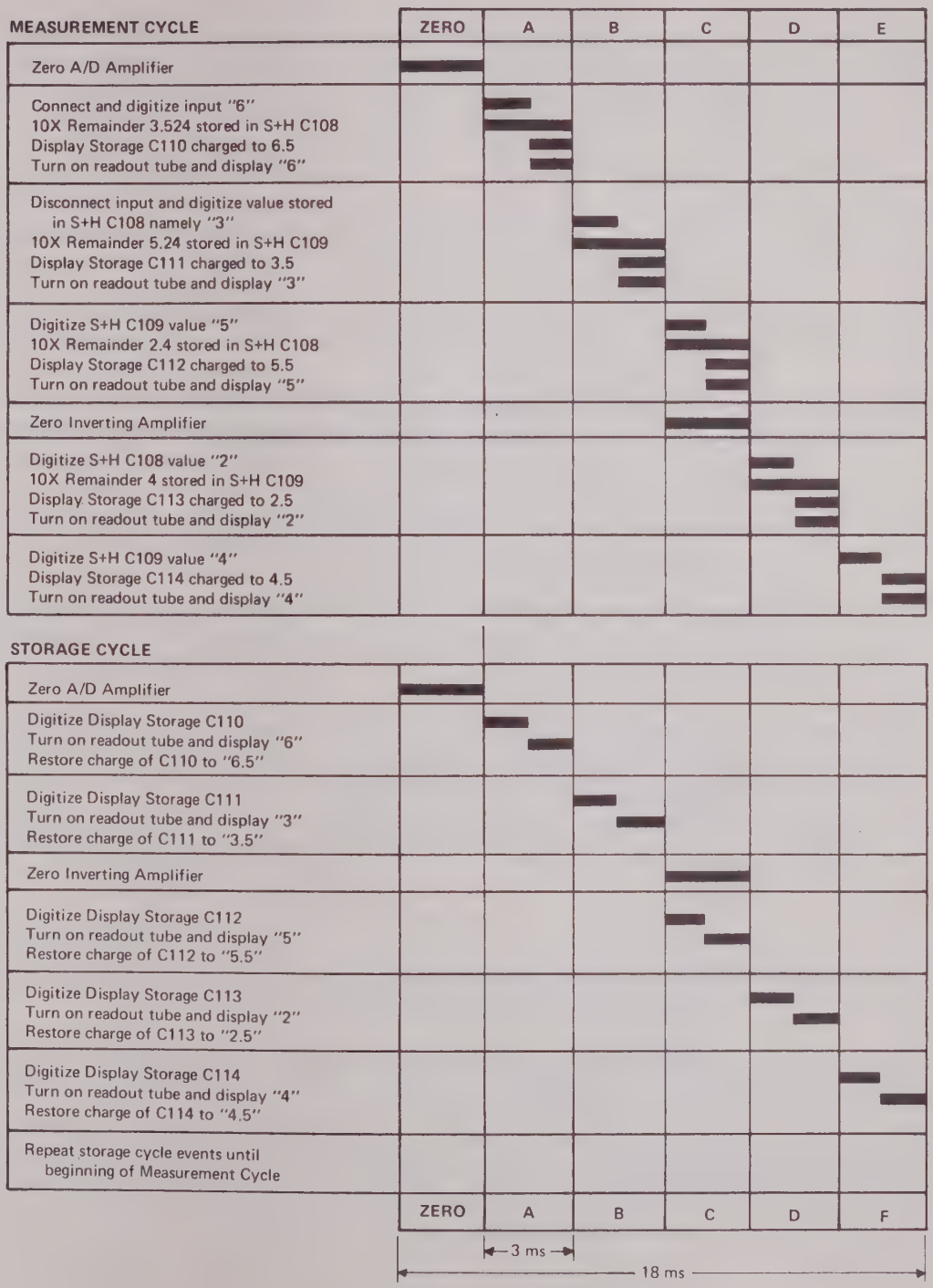

MEASUREMENT CYCLE
ZERO
A
B
C
D
E
Zero A/D Amplifier
Connect and digitize input "6"
10X Remainder 3.524 stored in S+H C108
Display Storage C110 charged to 6.5
Turn on readout tube and display "6"
Disconnect input and digitize value stored in S+H C108 namely "3"
10X Remainder 5.24 stored in S+H C109
Display Storage C111 charged to 3.5
Turn on readout tube and display "3"
Digitize S+H C109 value "5"
10X Remainder 2.4 stored in S+H C108
Display Storage C112 charged to 5.5
Turn on readout tube and display "5"
Zero Inverting Amplifier
Digitize S+H C108 value "2"
10X Remainder 4 stored in S+H C109
Display Storage C113 charged to 2.5
Turn on readout tube and display "2"
Digitize S+H C109 value "4"
Display Storage C114 charged to 4.5
Turn on readout tube and display "4"
STORAGE CYCLE
Zero A/D Amplifier
Digitize Display Storage C110
Turn on readout tube and display "6"
Restore charge of C110 to "6.5"
Digitize Display Storage C111
Turn on readout tube and display "3"
Restore charge of C111 to "3.5"
Zero Inverting Amplifier
Digitize Display Storage C112
Turn on readout tube and display "5"
Restore charge of C112 to "5.5"
Digitize Display Storage C113
Turn on readout tube and display "2"
Restore charge of C113 to "2.5"
Digitize Display Storage C114
Turn on readout tube and display "4"
Restore charge of C114 to "4.5"
Repeat storage cycle events until beginning of Measurement Cycle
ZERO
A
B
C
D
F
3 ms
18 ms

FIGURE 8.

The 6 State Shift Register (Figure 9), logic pack 4B, generate the six timing pulses used for timing in the instrument. These are the ZERO, A, B, C, D, and E pulses which are all clocked to the $\overline{H}$ pulses. This register is reset by the measure storage pulse from logic pack 16C at the end of each complete instrument cycle.

The 16 State Binary Counter (Figure 10) translates the pulses from the Current Controlled Oscillator into Binary Coded Decimal (BCD) output and controls the Ladder Switches and the Decoder Driver. It is reset at the beginning of each time period by the H pulse.

The 9's Catcher gate 9B operates from $\overline{W}$ and $\overline{Z}$ and A commands to stop the Current Controlled Oscillator.

The Conditional 11's Catcher, logic packs 8A and 19B operate to stop the 16 State Binary Counter in the A period.

The 12's Catcher operates in the A period and causes the instrument to up-range and the Over light to turn on.

Current Controlled Oscillator produces a pulse train that is proportional in repetition rate to the current being supplied. The oscillator is stopped in F time. It's output is fed to the 16 State Binary Counter to be translated into BCD output.

Analog Cycle Control provides gating functions that prevent the instrument from recycling until it completes it's present cycle, thus avoiding erroneous readings.

Manual Range Logic provides first priority of selection to the local front panel switches and provides the range commands as shown in Figure 11. Figure 12 shows the output as fed to the range flip-flop 18a and 18b.

Auto Range Logic operates when W and X from the 16 State Binary Counter and causes $\overline{UP}$ which initiates up ranging in the A period. $\overline{W}$ and $\overline{X}$ and $\overline{Y}$ and $\overline{Z}$ (zero) result in a $\overline{DN}$ signal which initiates down ranging in the A period. In addition when no Filter selection is made the instrument requires a settling time of about 10 ms. This is provided by R40 shunted by R41. When the Filter is selected R40 provides about 230 ms of delay for settling time.

E. Display (Schematic No. 4)

Display Circuits consist of the Function Lights, which are 5 volt lamps operated by the logic controls in the instrument and the relays and associated circuitry.

The Anode Strobing Control provides +190 volts to the readout tubes during the last half of each time period and lights each lamp in coordination with the proper time period.

Decoder Driver accepts the BCD output from the 16 State Binary Counter and translates it into decimal output, grounding the appropriate line to the readout tubes so that the tube will light when the +190 volts is applied by the Anode Strobing Control. Q41 operates the first readout tube whenever the count in A period reaches ten.

F. AC CONVERTER THEORY (Figure 13 and Schematic No. 6)

The AC Converter option for the 8300A converts input AC voltages, in four ranges, to DC for measurement by the A-D Converter. The output of the Converter is 0 to 12 VDC , which represents full scale.

PERIOD	SIX STATE SHIFT REGISTER				
	1A	1B	2C	2D	3E
ZERO	0	0	0	0	0
A	1	0	0	0	0
B	0	1	0	0	0
C	0	0	1	0	0
D	0	0	0	1	0
E	0	0	0	0	1

Figure 9.

RANGE	FLIP-FLOP	
	18a	18b
1	0	0
10	0	1
100	1	0
1000	1	1

Figure 12.

CCO PULSE COUNT	16 STATE BINARY COUNTER			
	7W	7X	6Y	6Z
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0

Figure 10.

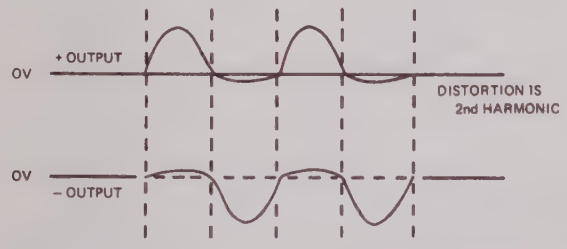
NOR GATES	RANGE									
	VAC & KΩ				VDC			MVDC		MΩ
	1	10	100	1000	10	100	1000	100	1000	10
12B	1	0	0	0	0	0	0	0	0	0
10D	0	1	0	0	1	0	0	0	0	0
10B	0	0	1	0	0	1	0	1	0	0
10C	0	0	0	1	0	0	1	0	1	0

Figure 11.

Zero adjust for the AC Option is located on the Buffer Board and is accessable from the front panel. Calibration of the assembly is made in the factory prior to shipment and the board may be placed in an instrument, the zero adjustment made and calibration checked. It should not be necessary to recalibrate the option after installation.

The block daigram, (Figure 13) is divided into two major parts. A wide band operational rectifier circuit where the ranging is accomplished and a DC difference (or subtracting) amplifier-intergrator where the rectifier output is filtered and amplified. The DC amplifier also provides the low source impedance required by the A-D Converter.

The operational rectifier circuit consists of an inverting transconductance amplifier and load resistor with feedback around them providing a loop gain of about 5×10^3 at mid band. The feedback is changed for ranging with reed relay switches. The input resistor is 1.11 megohms. This value shunted by the 10 megohm DC input divider is 1 megohm at the 8300A input. Q1 is a FET used as a source follower and Q2 provides a low impedance guard voltage which is used to bootstrap most of the capacity that otherwise would appear from the FET gate to common. The first two differential pairs are in a dual inline package. They and Q4 and Q5 develop the gain. Q3 and Q6 are current sources with such values that clipping due to overload is symmetrical. Changes in capacitor charges will be small and amplifier recovery time minimized. Q7 compensates for capacitance losses in the diodes at low levels. A symmetrical half wave rectifier placed between the amplifier and load resistor develops equal (+) and (—) DC voltages proportional to the amplifier output current. At full scale this current is near 2 ma. The two outputs have the following wave forms.



The DC difference amplifier-integrator filters the waveform and amplifies the DC difference between them by about 10 times for measurement by the A-D Converter. Three section filtering, which cannot be observed on the readout when the input voltage is at full scale and above 100 Hz. Below 100 Hz a few digits respond to the ripple. At 50 Hz the readout excursions do not exceed ±.01% of reading and at 30 Hz are within ±.05% of reading. Q9 is a dual FET which is used for the input of the low drift DC amplifier. Further gain for the DC amplifier is developed by a monolithic operational amplifier to produce a total loop gain at DC of about 5×10^5.

G. MILLIVOLT/OHMS CONVERTER THEORY (Figure 14, 15 and Schematic No. 7)

As the name implies, the Millivolt/Ohms Converter performs two functions. The use of the converter in the 8300A allows measurement of resistance over five ranges and provides two DC voltage ranges in addition to the three ranges offered by the basic instrument. The five resistance ranges are 1 KΩ, 100 KΩ, 1000 KΩ and 10 MΩ. The two additional DC voltage ranges are 100 mv and 100 mv. As with the basic instrument, the above ranges have a 20% over-range capability. Thus the 1 KΩ range will accurately read to 1.19999 KΩ.

This converter can be thought of as two converters. One converter is a chopper amplifier which provides a DC amplification of an unknown voltage prior to A-D Conversion. Signal gain is necessary if a 100 mv signal on the 100 mv range is to provide a corresponding 10V DC signal into the A-D Converter.

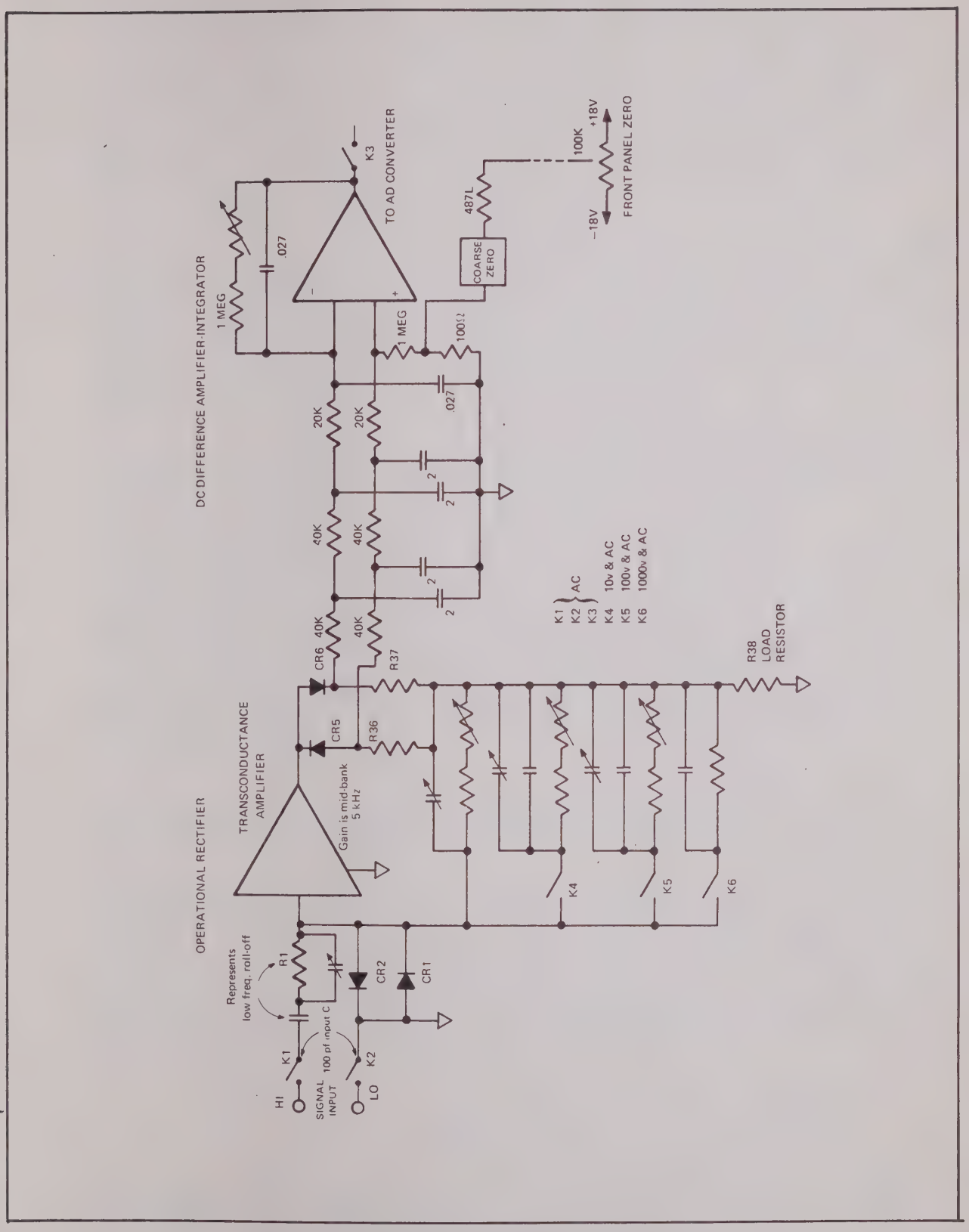


FIGURE 13. BLOCK DIAGRAM AC CONVERTER

The other converter in the Millivolt/Ohms Converter is a precision current ladder which, in conjunction with the Buffer amplifier, provides a known current through the resistor to be measured. Refering to Figure 14, a MOSFET chopper is used across the summing junctions of an operational amplifier. The signal developed due to the chopping action is amplified and presented through a capacitor to a half-wave synchronous demodulator. The Demodulator output is sent to a high gain (at DC) operational amplifier connected as an integrator. The integrator output is brought to the MOSFET chopper in a manner to insure negative feed-back. An input RC network provides input filtering to prevent beat frequency products at the amplifier output and balanced AC impedances for the chopper.

The use of the MOSFET chopper as shown allows the spike developed due to capacitive coupling from gate drive to channel to become a common mode signal for a high common mode rejection operational amplifier. Balanced AC impedances at the chopper provide cancellation effect of the offset current and voltage due to the capacitive spike. The new result is a chopper amplifier capable of operating at a fairly high frequency with small voltage and current offsets, and with spikes of low enough value to keep the AC amplifier from saturating. The above operation is achieved without large adjustments for spike compensation.

The overall millivolt amplifier can be considered to be a high DC gain operational amplifier utilizing potentiometric feedback to provide programmed gains of x10 or x100 and very high input impedance at DC. The A-D Converter follows the millivolt converter to provide digitization of the amplified analog representation of the input signal to the millivolt converter.

The current ladder is connected to the Buffer and the millivolt converter as shown in Figure 15. The inverting terminal of the Buffer amplifier is held very near analog common by the feedback connection of the unknown resistance. Because the inverting terminal is held near ground, and because the input current to the Buffer is small, the current through the unknown resistor is set by the reference voltage (7 volts) and the resistor selected by the range command. For the three upper KΩ ranges, the output of the buffer is presented to the A-D Converter. Thus since the A-D Converter digitizes 11.9999 as full scale, then that voltage must represent full scale on the KΩ ranges. Simple arithmetic shows us that the sampling currents for the three ranges to be 1 ua, 10 ua, and 100 ua respectively.

For the 1 KΩ and the 10 KΩ range, smaller full scale voltages are used in order to keep load dissipation down. Thus, on these two ranges, the millivolt converter is used to amplify the voltage across the unknown resistor and present the amplified voltage to the A-D Converter.

In addition to providing smaller full scale impressed voltages in the lower two resistance ranges, the use of the millivolt converter allows a "modified four terminal" resistance measurement to be made. The term "modified four terminal" is used because the technique employed requires a small current in one of the sense lines that would not be present in a true four terminal resistance measurement. The sense current magnitude is determined by the voltage impressed on the resistor to be measured divided by R_i. By example, if the sense line resistance is 10Ω, then the error due to the sense current can be computed roughly as follows:

$$\text{Error} = \frac{10\Omega}{R_i} = \frac{100\Omega}{1000\Omega} = 10^{-4} \text{ or } 100 \text{ ppm of reading.}$$

If a two terminal reading were made at the 1 KΩ level with a 10Ω resistance in the hook-up wires, the error would be about 10,000 ppm. The improvement in performance using a "modified four terminal" measurement is obvious.

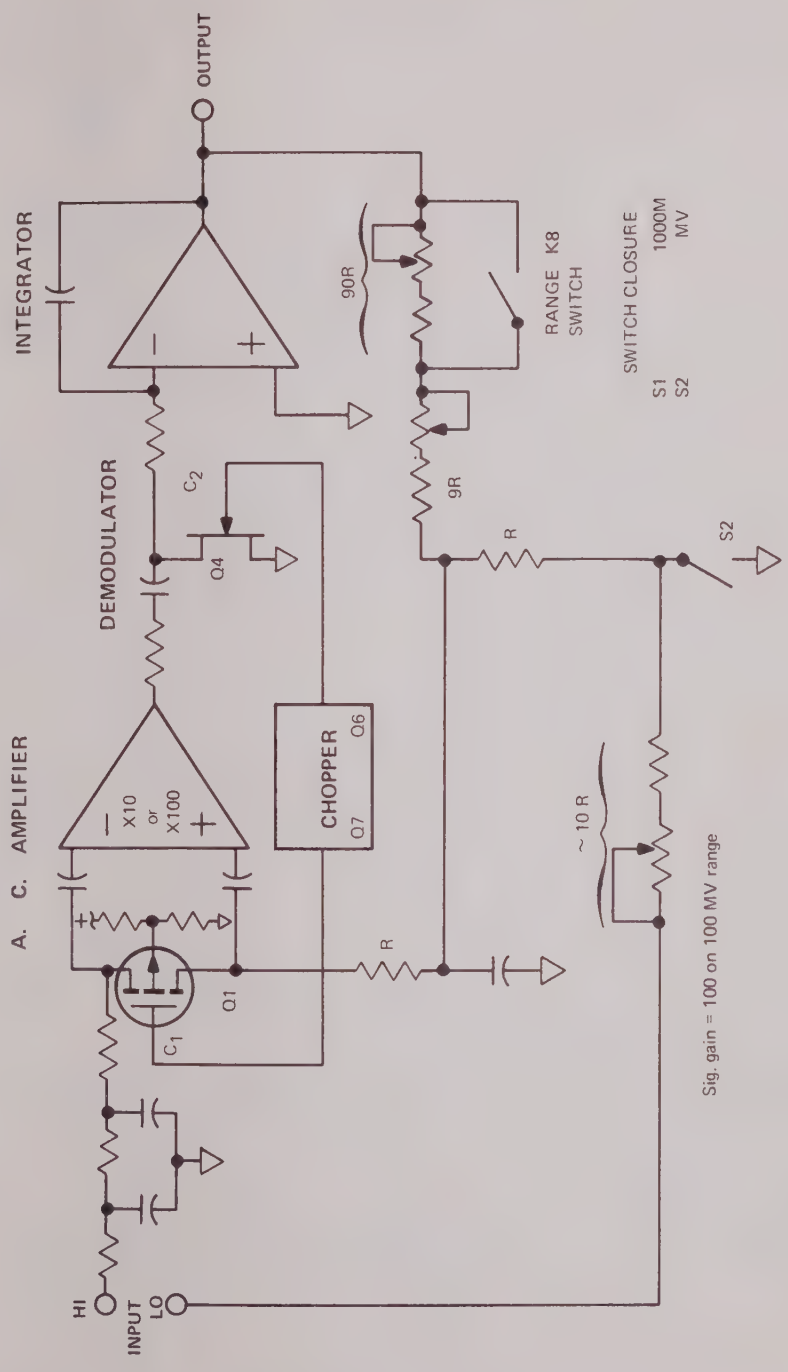
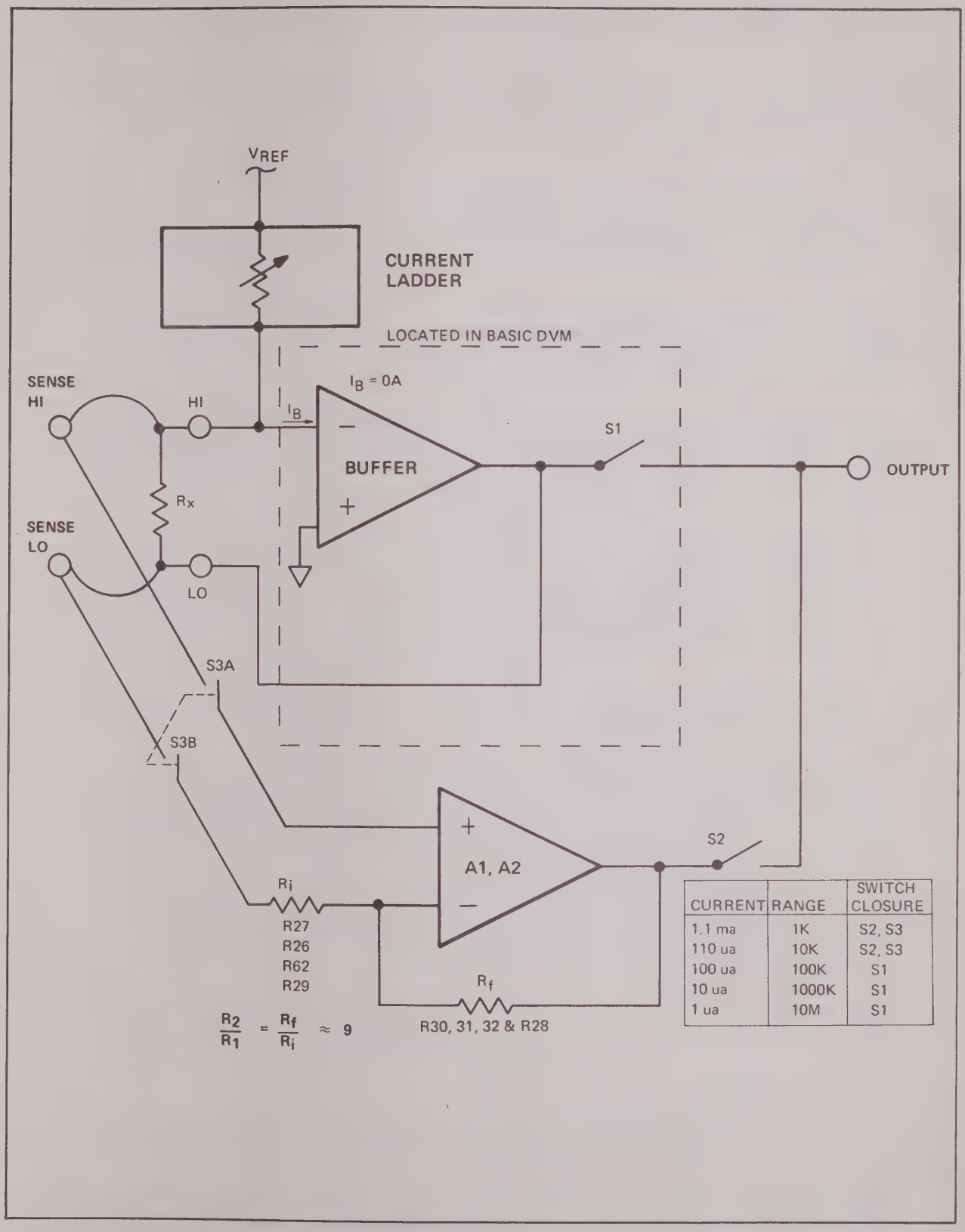


FIGURE 14. BLOCK DIAGRAM OF MILLIVOLT CONVERTER



CURRENT	RANGE	SWITCH CLOSURE
1.1 ma	1K	S2, S3
110 ua	10K	S2, S3
100 ua	100K	S1
10 ua	1000K	S1
1 ua	10M	S1

FIGURE 15. BLOCK DIAGRAM OF OHM CONVERTER

H. EXTERNAL REFERENCE THEORY (Figure 16, 17, 18, 19 and Schematic No. 10)

The 8300A input terminal for VDC measurements is the input to the A-D Converter and therefore, will have a maximum voltage of ±12v with respect to the instrument common, Figure 16. Since it may be necessary to connect the common of the input to the common of External Reference input and the External Reference output common is instrument common, a means of isolating the commons becomes necessary.

Refer to Figure 17. Switches S1 and S2 are arranged so that when one set is closed, the other is open. S1 is closing during a non-critical (the A-D ZERO time) portion of the measurement cycle and allowed to charge to the voltage, E_R. When S2 is closed, the output of A_1 goes to E_R satisfying the voltage follower.

Refering to the circuit schematic, A2 is the S1 of the block diagram, Q4 and Q5 the switch, S2. A matched pair of J-FETS followed by a monolithic amplifier made up the high input impedance voltage follower. Q8 and R17 is a constant current source for the J-FET amplifiers. Frequency compensation is provided by the C4, C5 and C6.

The reference voltage is sensed through R18 from the A-D Amplifier board compensating for line drops. Low sense (Reference Common) also comes from the main board. CR7 and CR8 provide feedback to the voltage follower when the reed relay, S1 is open, keeping the amplifier output within 0.5v of the voltage of C8 to control the gate drive for Q4.

C7 forms an RC filter with the input driver giving improved noise performance. C9 provides an input impedance to the voltage follower during the time the FET switches, Q5 and Q6 are open.

Q1 and Q2 are gate drivers for the J-FET switches. Using the reference voltage for the collector supply of Q2 assures that the gate signal of Q4 never goes positive with respect to its terminal. The gate of Q5 is clamped to within .2v of common by diode CR6. R13 limits the current through CR6. C2 compensates for the capacity of CR6.

A voltage of as much as ±12.0v with respect to reference common will appear at the low terminal of EX REF input when the EX REF common is tied to the instrument input common.

A schematic showing the voltage distribution is shown in Figure 25. The MOS FET's used are P-channel enhancement mode devices. A negative gate voltage of 10v or more is needed to insure that the transistor is on. 0v or a positive gate voltage turns the transistor off. Refering to Figure 18, the upper switch needs a minimum of −15v to turn on and a maximum of 19v to turn off. The bottom switch needs a minimum of −22v to turn on and a maximum of 12v to turn off.

The MOS FET gate driver is redrawn in Figure 19 showing the peak voltages. When the transistor is saturated, CR1 is back biased. When the transistor is cutoff, C3 charges to 8v because of the 12v drop across the zener. This voltage subtracts from the collector voltage giving the voltage shown.

When the EXT REF control line is 5v (the EXT REF button pushed) −18v is applied to the local Disable line with Q10 and Q12.

Input protection is provided with CR4, CR5 and R12.

IV. TROUBLESHOOTING AND ANALYSIS (Figure 20. 21, 22, and 23)

1. The following is a list of recommended test equipment that is required to test and calibrate the 8300A. If the recommended equipment is not available, other equipment which meets the required specifications may be used.

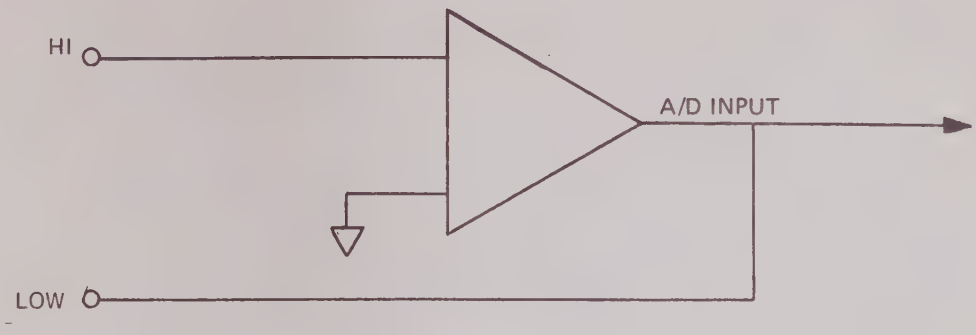


FIGURE 16.

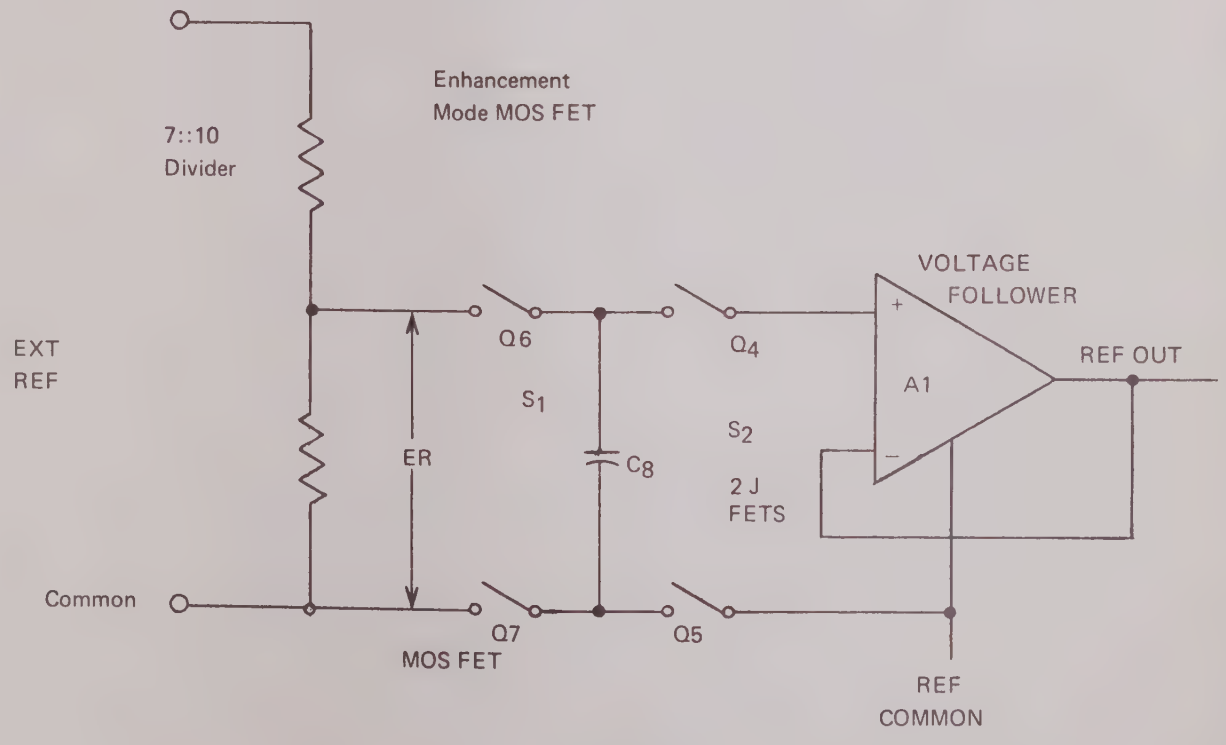


FIGURE 17.

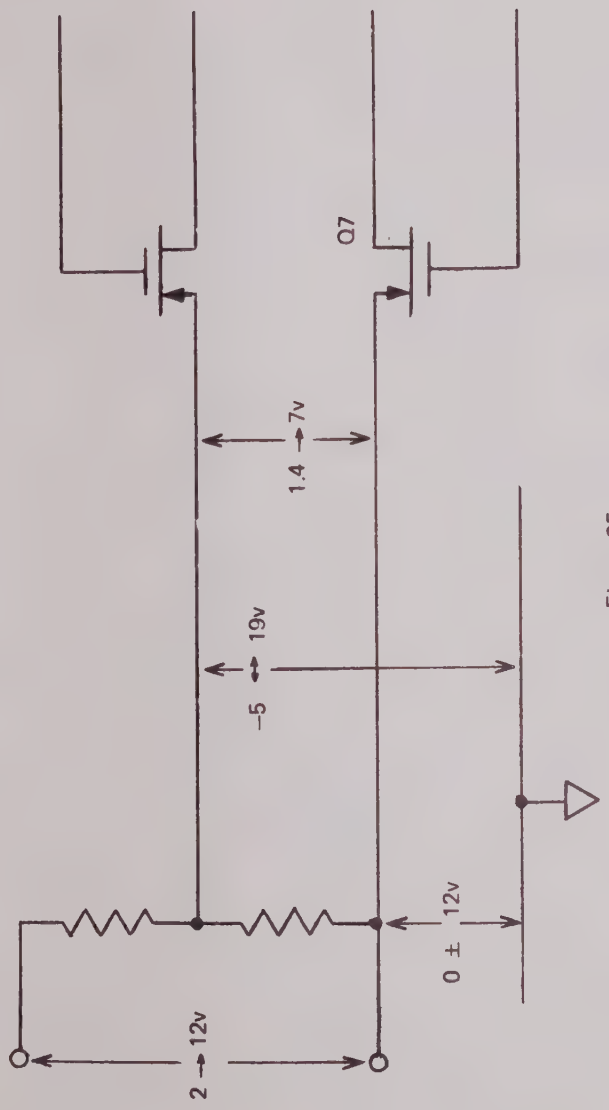


FIGURE 18.

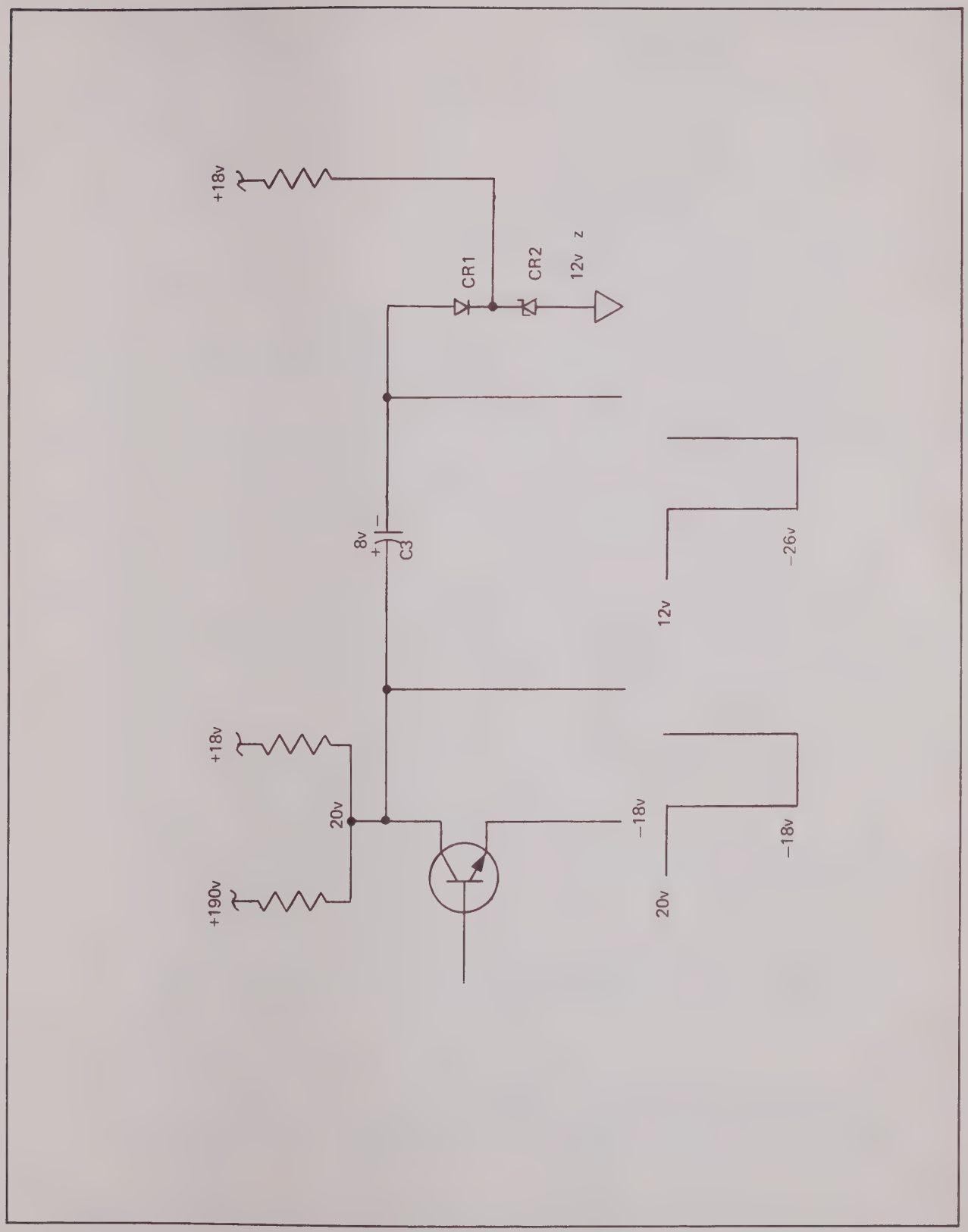


FIGURE 19.

EQUIPMENT NOMENCLATURE	RECOMMENDED EQUIPMENT
Oscilloscope	Tektronix Model 547
Oscilloscope Plug-In	Tektronix Model 1A1
Oscilloscope Probes	Tektronix Model P6010
DC Voltage Source	Fluke Model 343A DC Voltage Calibrator
AC Voltage Source	HP Model 745A
Differential Voltmeter	Fluke Model 885A

2. An excellent source of synchronization for the Oscilloscope may be obtained by using the $\overline{\text{ZERO}}$ signal that is available at TP4 or TP108. By proper adjustment of the horizontal trace time it is possible to see all of the other timing pulses in their proper relationship.
3. With the covers and shields removed it is reasonable to expect to see more noise in the output as the 8300A is quite sensitive to interference when these protections are removed.
4. Figure 20 gives the general location of the various sections of the instrument.
5. Figure 21 locates the various test points (TP) and is a guide to the location and index of the logic packs.
6. All voltage measurements and pulse observations should be made with reference to the instrument signal ground which is available at TP3 and TP109.
7. Figure 22 gives a step by step procedure for troubleshooting the Display section of the 8300A.
8. Figure 23 gives an excellent step by step procedure for troubleshooting the analog circuitry.
9. Many cases of trouble can be analized from the operation and readout observations of the instrument. As examples the following are presented:

   a. Readout is in error only in the negative polarity.

      It is reasonable to assume that the trouble is located in either the polarity FET switch- or in the Inverting Amplifier since these paths are utilized only in the negative polarity.

   b. More than one digit displayed in the readout tubes.

      The Decoder Driver is the most likely source of this trouble. If ground potential is supplied to more than one of the decimal lines to the readout tubes, multiple numbers will light. There remains the possibility that the Anode Strobing circuits are mal-functioning.

   c. Only the first digit is displayed, all others read 0.

      It is reasonable to assume that the remainders are not being stored in the Sample and Hold circuitry. This can be caused by a failure in the FET switches or a short in the storage capacitors. It is also possible that two significant digits will be developed and displayed.

   d. First digit reads higher than the input voltage and all other digits read 0.

      Count the pulses from the Current Controlled Oscillator. If correct check the BCD

output of the A4 Counter. If the BCD output is correct the Ladder output voltage could be too high.

e. A large signal of either polarity is needed to cause a reading of other than 0.0000.

The A-D Auto Zeroing circuit, Q117 and Q118 should be checked.

f. None of the readout tubes lighted.

Check the +5 and the +190 volt supplied.

10. The basic instrument may be checked by applying a 0 to 12 volt DC signal at the input to the Inverting Amplifier. This should cause the instrument to display the voltage applied.

11. By applying a jumper between TP6 and TP201 the instrument can be made to sample continuiously. This procedure can be used to locate trouble in the Storage circuitry.

12. The logic section of the instrument can be broken up into several independent sections for trouble analysis as follows:

a. Master Clock

Check the output of Q45, then look for the F, $\overline{H}$ and $\overline{ZERO}$ pulses.

b. Six State Shift Register.

Check for the presence of the A, B, C, D, and E pulses and their inversions.

c. Check the output of the Current Controlled Oscillator and the BCD output of the 16 State Binary Counter.

d. Display readout tubes.

Anodes and Anode Strobing circuitry.
Cathode circuits including the Decoder Driver.
Decimal lines.

e. Function Indicators.

+5 volt incandescent lights and associated circuitry.

f. Sample Oscillator should be checked for output.

g. Figures C through G and the Picture waveforms attached will be of additional assistance in locating troubles.

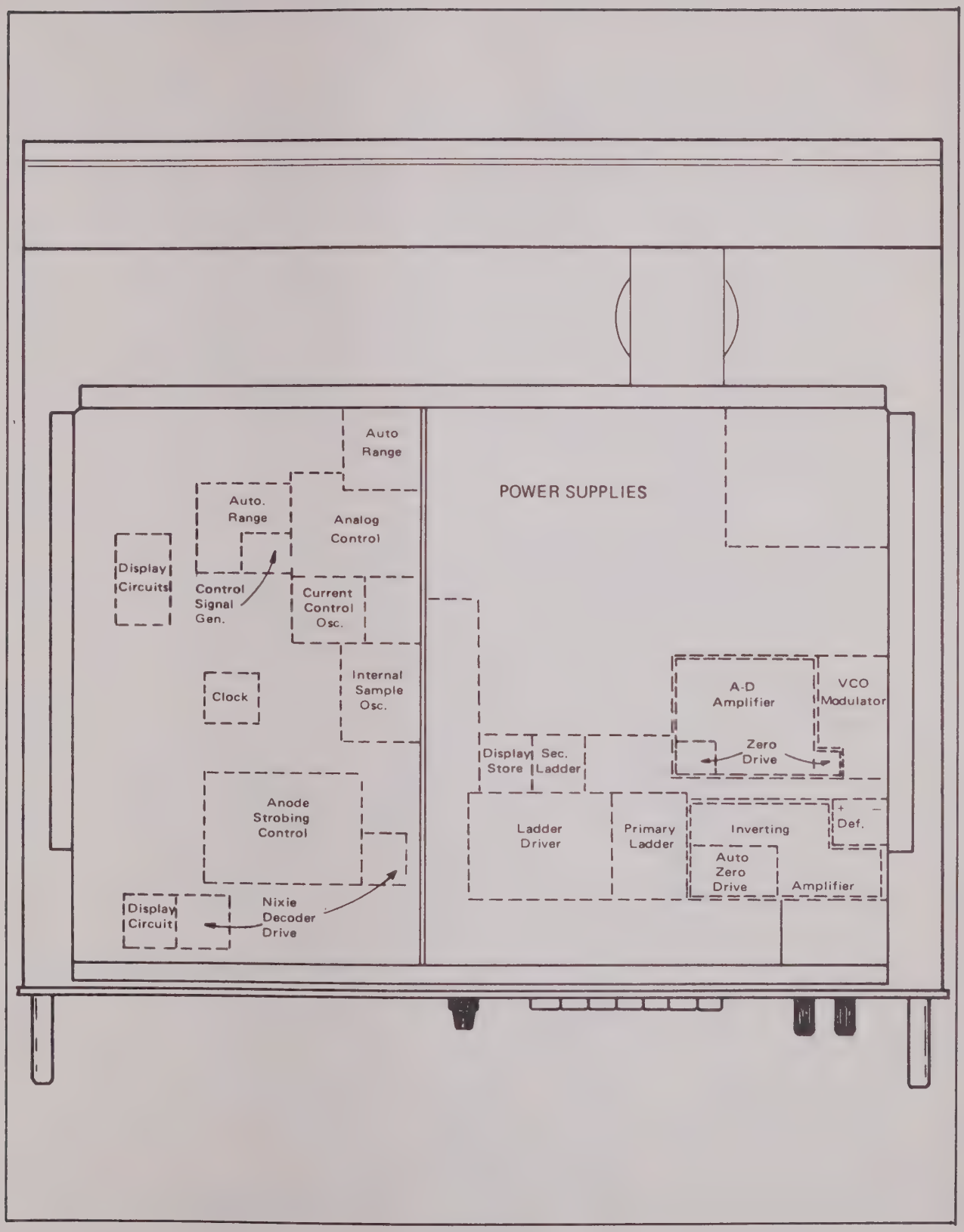

Auto
Range
POWER SUPPLIES
Auto.
Range
Analog
Control
Display
Circuits
Control
Signal
Gen.
Current
Control
Osc.
Internal
Sample
Osc.
Clock
A-D
Amplifier
VCO
Modulator
Zero
Drive
Display
Store
Sec.
Ladder
Anode
Strobing
Control
Ladder
Driver
Primary
Ladder
Inverting
+
−
Def.
Auto
Zero
Drive
Amplifier
Display
Circuit
Nixie
Decoder
Drive

FIGURE 20.

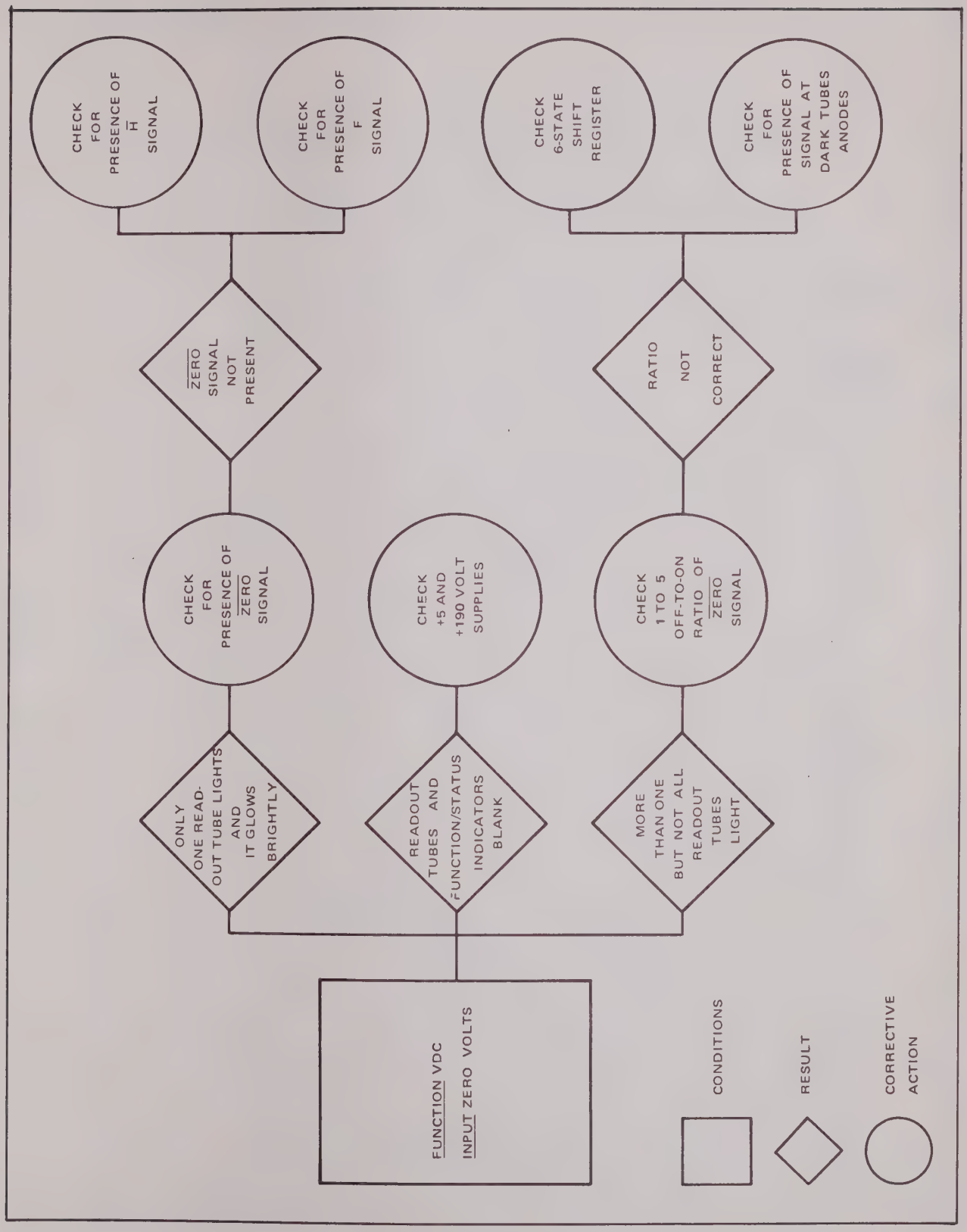

FUNCTION VDC
INPUT ZERO VOLTS
ONLY ONE READ-OUT TUBE LIGHTS AND IT GLOWS BRIGHTLY
READOUT TUBES AND FUNCTION/STATUS INDICATORS BLANK
MORE THAN ONE BUT NOT ALL READOUT TUBES LIGHT
CHECK FOR PRESENCE OF ZERO SIGNAL
CHECK +5 AND +190 VOLT SUPPLIES
CHECK 1 TO 5 OFF-TO-ON RATIO OF ZERO SIGNAL
ZERO SIGNAL NOT PRESENT
RATIO NOT CORRECT
CHECK FOR PRESENCE OF H SIGNAL
CHECK FOR PRESENCE OF F SIGNAL
CHECK 6-STATE SHIFT REGISTER
CHECK FOR PRESENCE OF SIGNAL AT DARK TUBES ANODES
CONDITIONS
RESULT
CORRECTIVE ACTION

FIGURE 21.

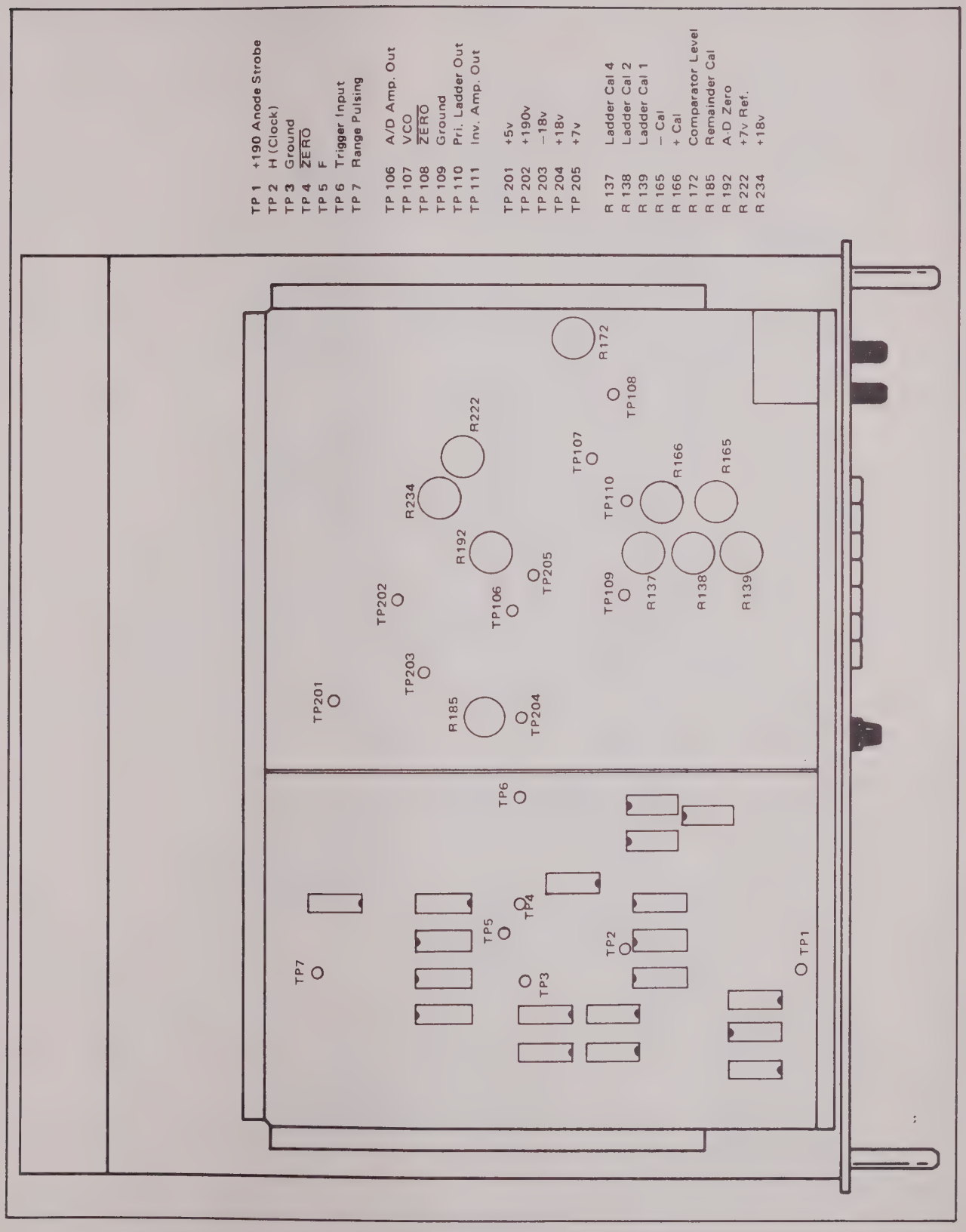

TP 1 +190 Anode Strobe
TP 2 H (Clock)
TP 3 Ground
TP 4 ZERO
TP 5 F
TP 6 Trigger Input
TP 7 Range Pulsing
TP 106 A/D Amp. Out
TP 107 VCO
TP 108 ZERO
TP 109 Ground
TP 110 Pri. Ladder Out
TP 111 Inv. Amp. Out
TP 201 +5v
TP 202 +190v
TP 203 −18v
TP 204 +18v
TP 205 +7v
R 137 Ladder Cal 4
R 138 Ladder Cal 2
R 139 Ladder Cal 1
R 165 − Cal
R 166 + Cal
R 172 Comparator Level
R 185 Remainder Cal
R 192 A-D Zero
R 222 +7v Ref.
R 234 +18v
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP201
TP202
TP203
TP204
TP205
TP106
TP107
TP108
TP109
TP110
R185
R192
R234
R222
R137
R138
R139
R165
R166
R172

FIGURE 22.

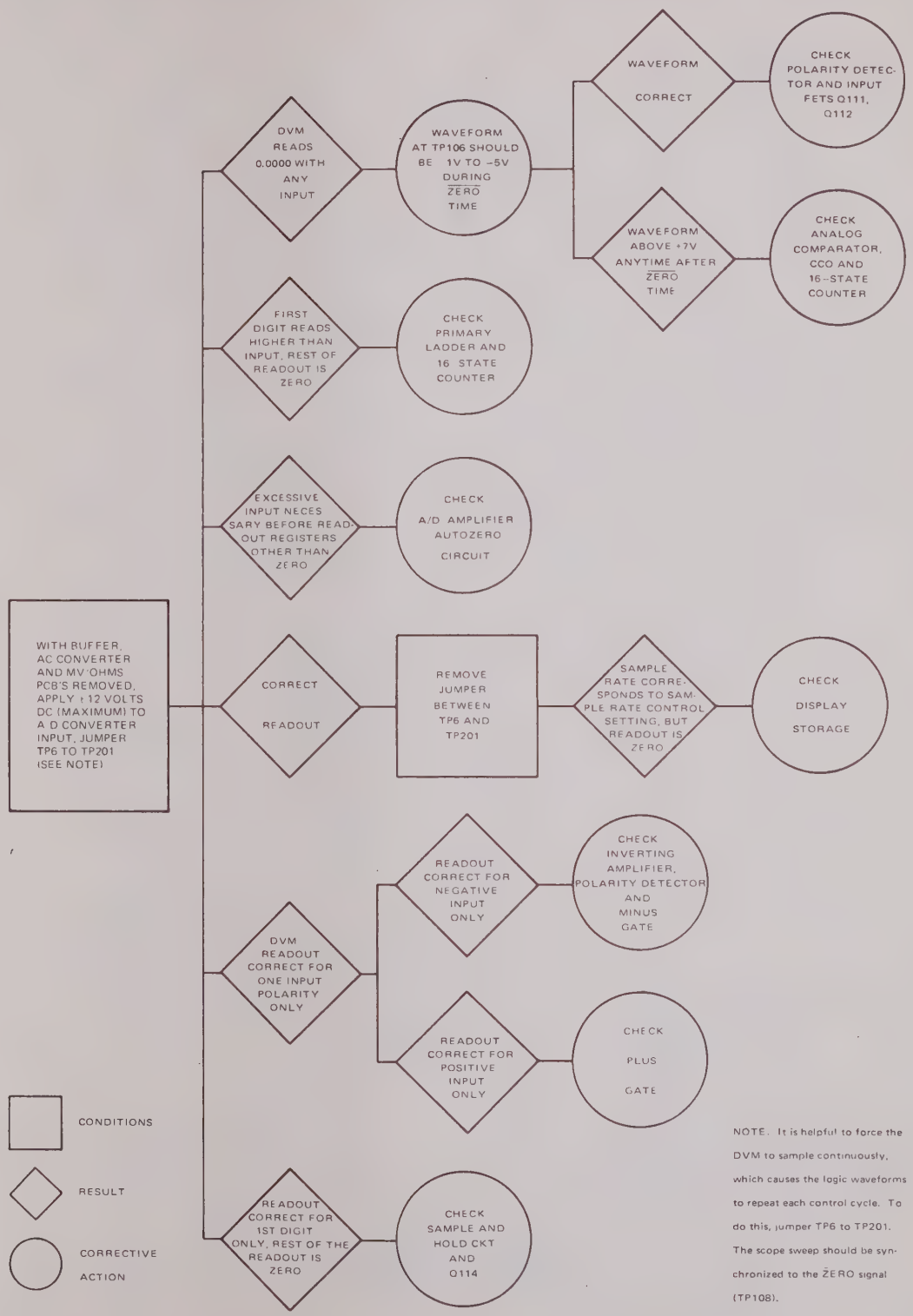
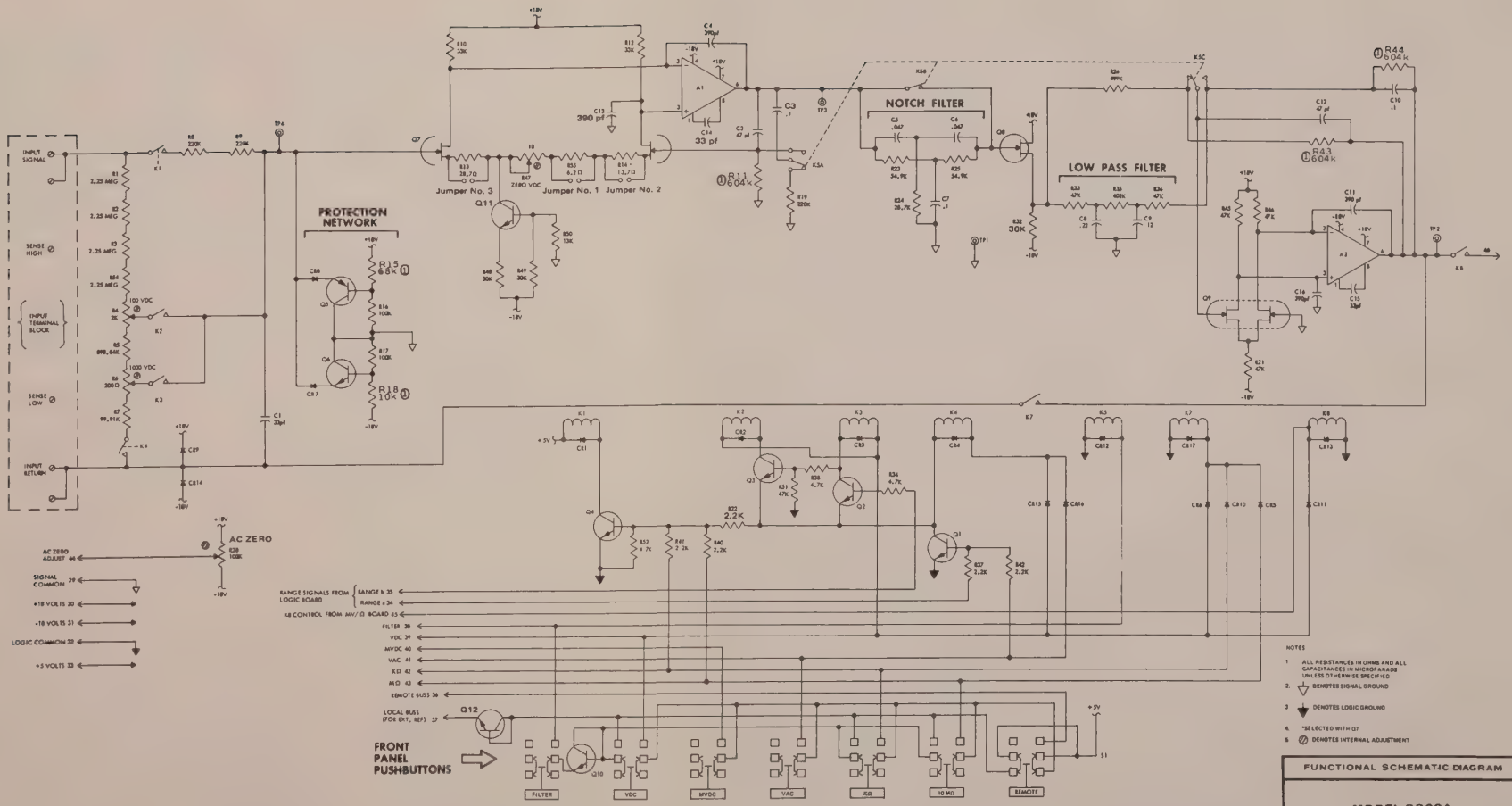

WITH BUFFER, AC CONVERTER AND MV-OHMS PCB'S REMOVED, APPLY ± 12 VOLTS DC (MAXIMUM) TO A-D CONVERTER INPUT, JUMPER TP6 TO TP201 (SEE NOTE)
CORRECT READOUT
REMOVE JUMPER BETWEEN TP6 AND TP201
SAMPLE RATE CORRESPONDS TO SAMPLE RATE CONTROL SETTING, BUT READOUT IS ZERO
CHECK DISPLAY STORAGE
DVM READS 0.0000 WITH ANY INPUT
WAVEFORM AT TP106 SHOULD BE 1V TO -5V DURING ZERO TIME
WAVEFORM CORRECT
CHECK POLARITY DETECTOR AND INPUT FETS Q111, Q112
WAVEFORM ABOVE +7V ANYTIME AFTER ZERO TIME
CHECK ANALOG COMPARATOR, CCO AND 16-STATE COUNTER
FIRST DIGIT READS HIGHER THAN INPUT, REST OF READOUT IS ZERO
CHECK PRIMARY LADDER AND 16 STATE COUNTER
EXCESSIVE INPUT NECESSARY BEFORE READOUT REGISTERS OTHER THAN ZERO
CHECK A/D AMPLIFIER AUTOZERO CIRCUIT
DVM READOUT CORRECT FOR ONE INPUT POLARITY ONLY
READOUT CORRECT FOR NEGATIVE INPUT ONLY
CHECK INVERTING AMPLIFIER, POLARITY DETECTOR AND MINUS GATE
READOUT CORRECT FOR POSITIVE INPUT ONLY
CHECK PLUS GATE
READOUT CORRECT FOR 1ST DIGIT ONLY, REST OF THE READOUT IS ZERO
CHECK SAMPLE AND HOLD CKT AND Q114
CONDITIONS
RESULT
CORRECTIVE ACTION
NOTE. It is helpful to force the DVM to sample continuously, which causes the logic waveforms to repeat each control cycle. To do this, jumper TP6 to TP201. The scope sweep should be synchronized to the ZERO signal (TP108).

FIGURE 23.



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ▽ DENOTES SIGNAL GROUND
3. ▼ DENOTES LOGIC GROUND
4. *SELECTED WITH Q7
5. Ⓐ DENOTES INTERNAL ADJUSTMENT

CHANGES:
① For S/N 123 thru 1495: R11, R43, & R44 were 1Megohm. R15 & R18 were 220k.

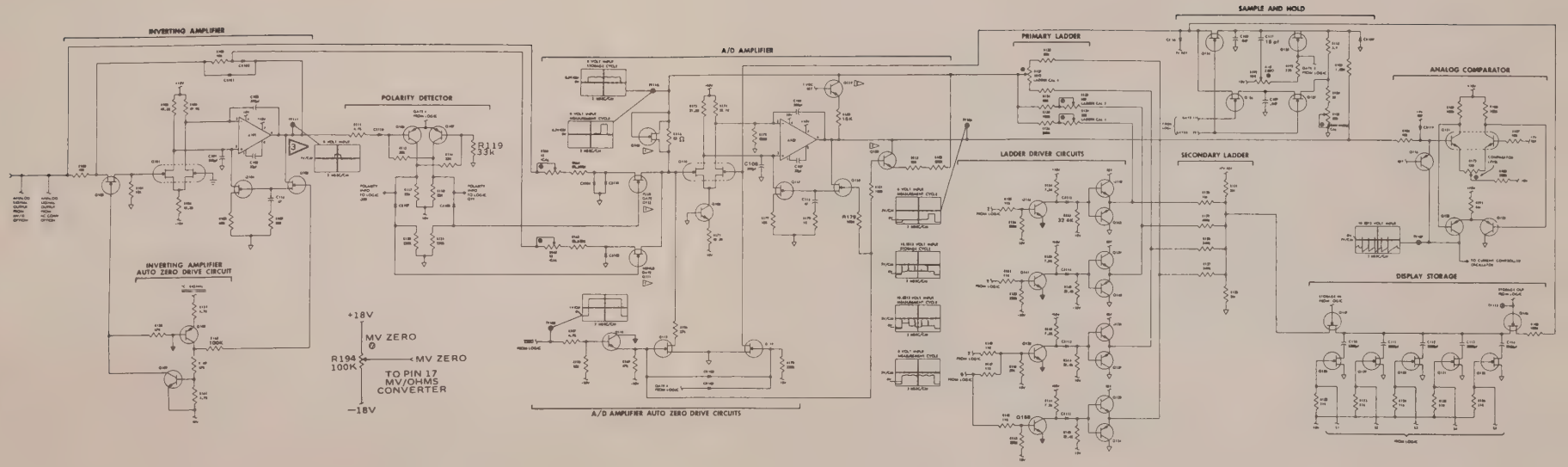
FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A BUFFER

SCHEMATIC NO 1

SER NO 123 & ON	REV C

FLUKE JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle, Washington 98133



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. 1 DENOTES MATCHED SET
3. 2 DENOTES SELECTED TRANSISTOR
4. DENOTES SIGNAL GROUND
5. DENOTES LOGIC GROUND
6. DENOTES INTERNAL ADJUSTMENT
7. 3 STEP POLARITY MAY BE EITHER POSITIVE OR NEGATIVE, DEPENDING ON Q104 CHARACTERISTICS.

FUNCTIONAL SCHEMATIC DIAGRAM

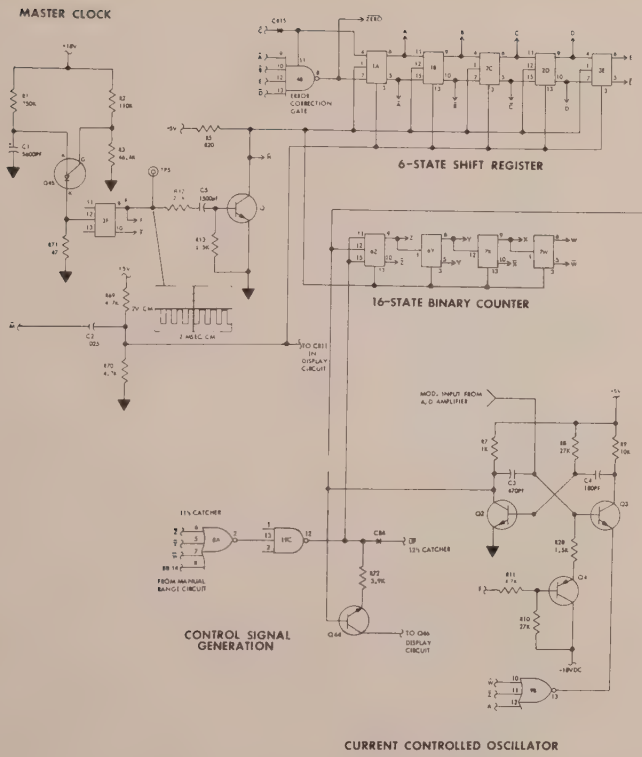
MODEL 8300A
A/D CONVERTER

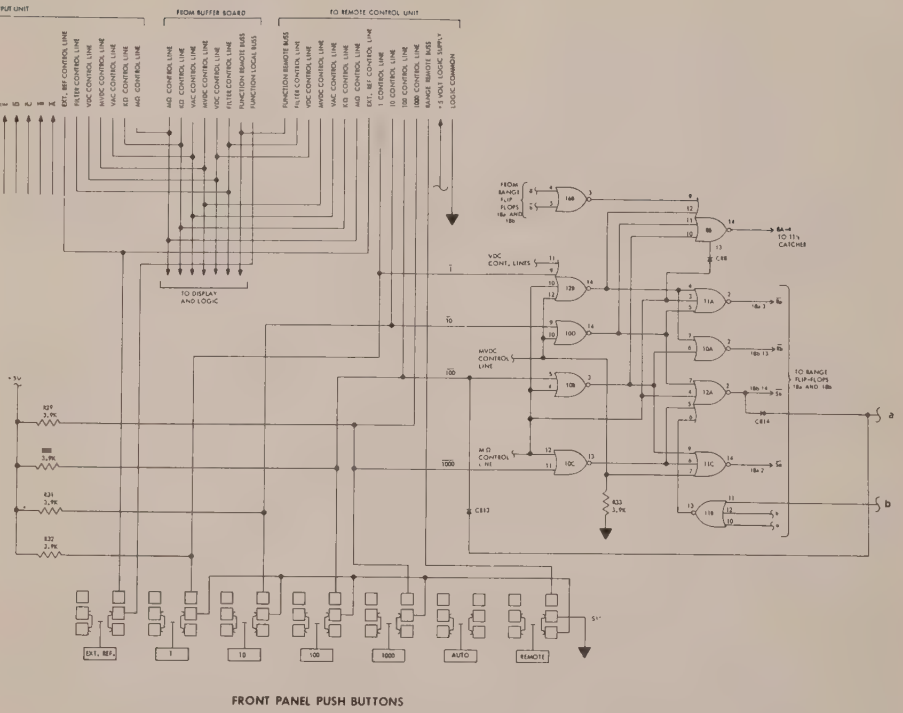
SCHEMATIC NO 2

SER NO 123 & ON

REV d

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle Washington 98133

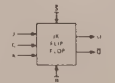




FRONT PANEL PUSH BUTTONS

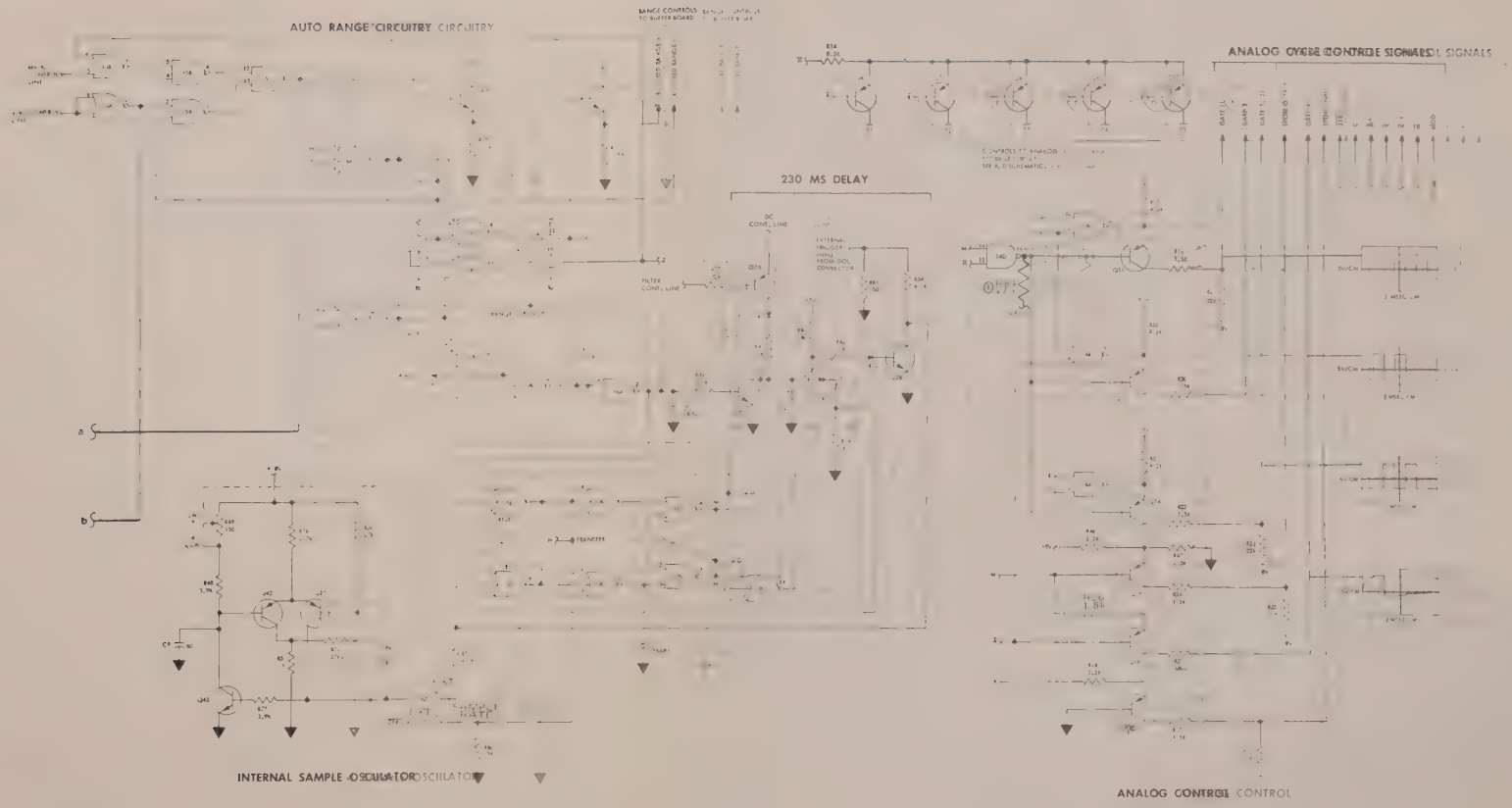
NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. FLIP FLOP KEY:



3. ▼ DENOTES LOGIC GROUND
4. ★ SWITCHES COMPRISING S1 SHOWN IN OFF (NON-DEPRESSED) POSITION.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DVM LOGIC & CONTROL	
SCHEMATIC NO. 3 SHEET 1	
SER NO 123 & ON	REV C
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



CHANGES:
① R84 added at S/N 1750 and on 250 and

FUNCTIONAL SCHEMATIC DIAGRAM

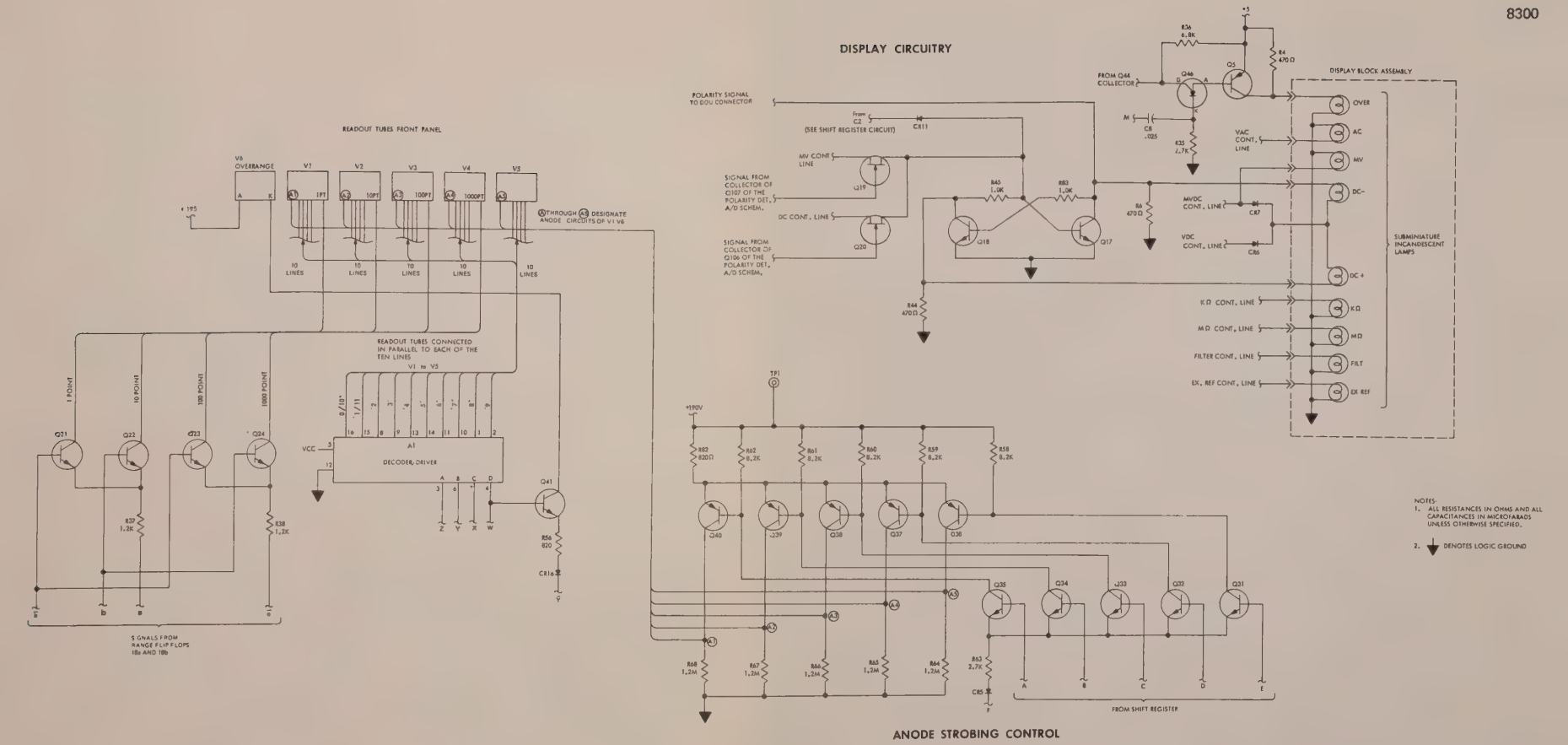
MODEL 8300A
DVM LOGIC & CONTROL

SCHEMATIC NO. 3 SHEET 2

REV d

FLUKE JOHN FLUKE MFG. CO., INC.

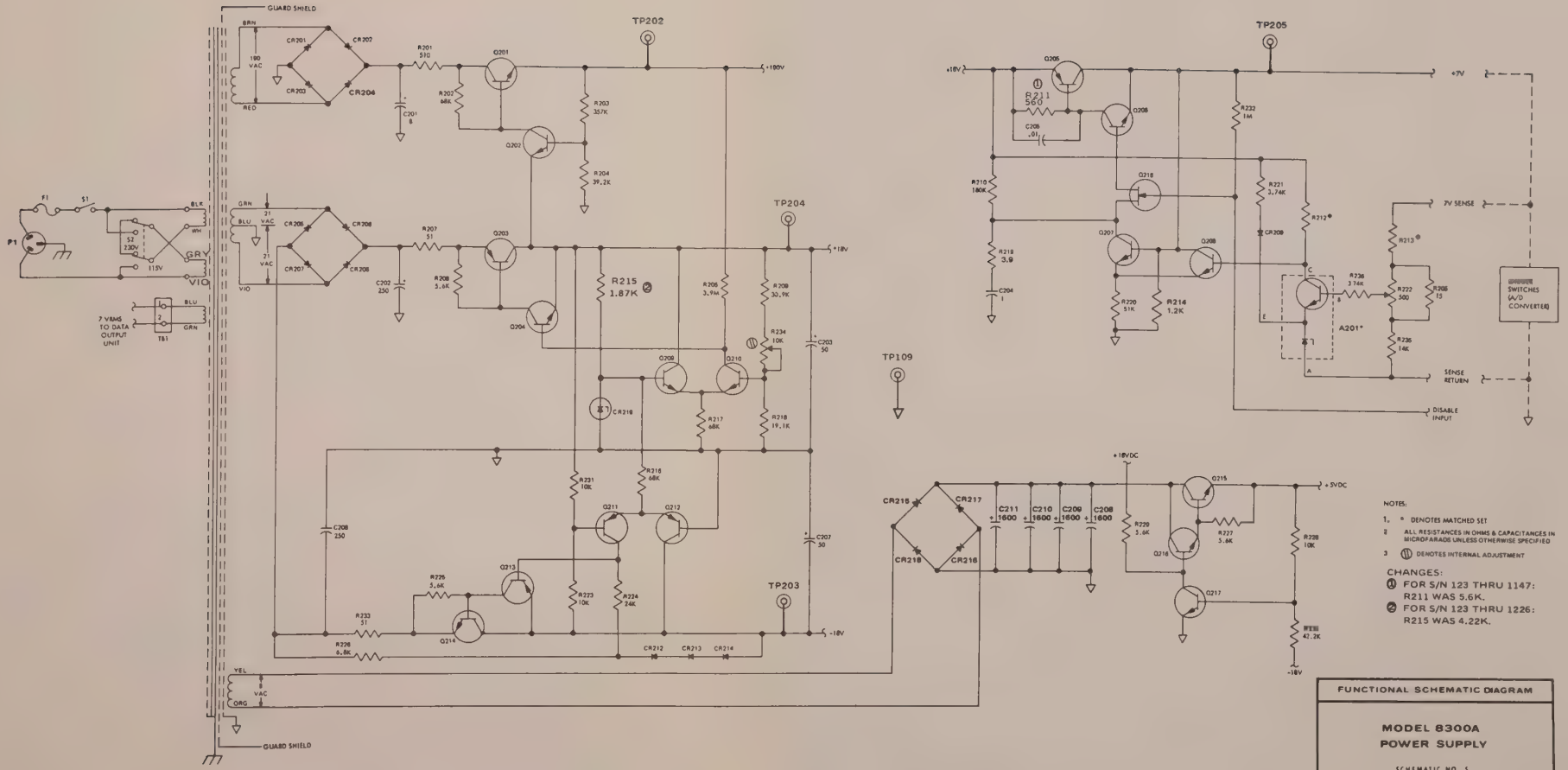
SEE SHEET 1 FOR NOTES



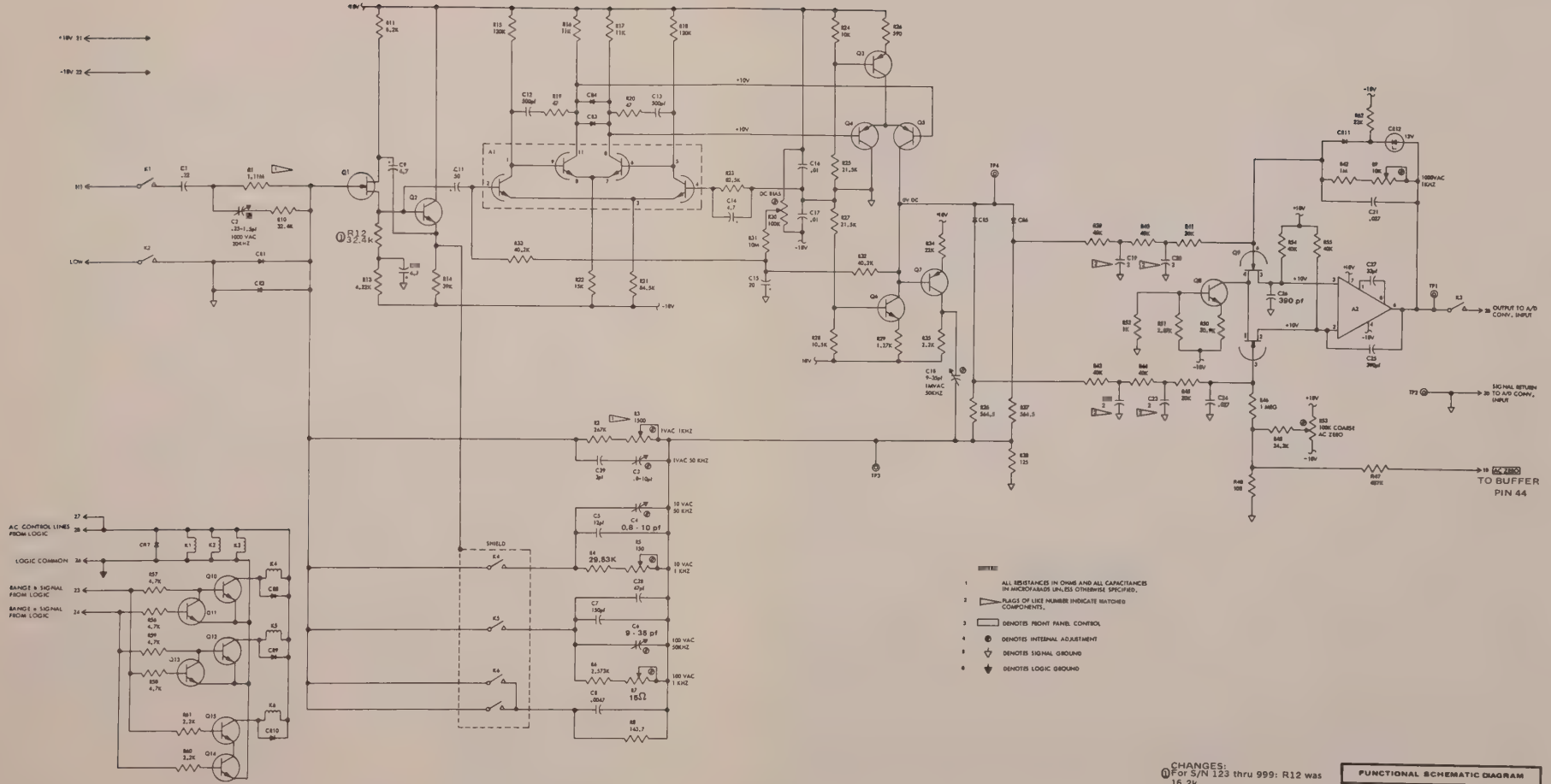
ANODE STROBING CONTROL

NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⏚ DENOTES LOGIC GROUND

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DISPLAY SCHEMATIC NO 4	
SER NO 123 & ON	REV C
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle Washington 98133	



FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A POWER SUPPLY	
SCHEMATIC NO 5	
SER NO 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	

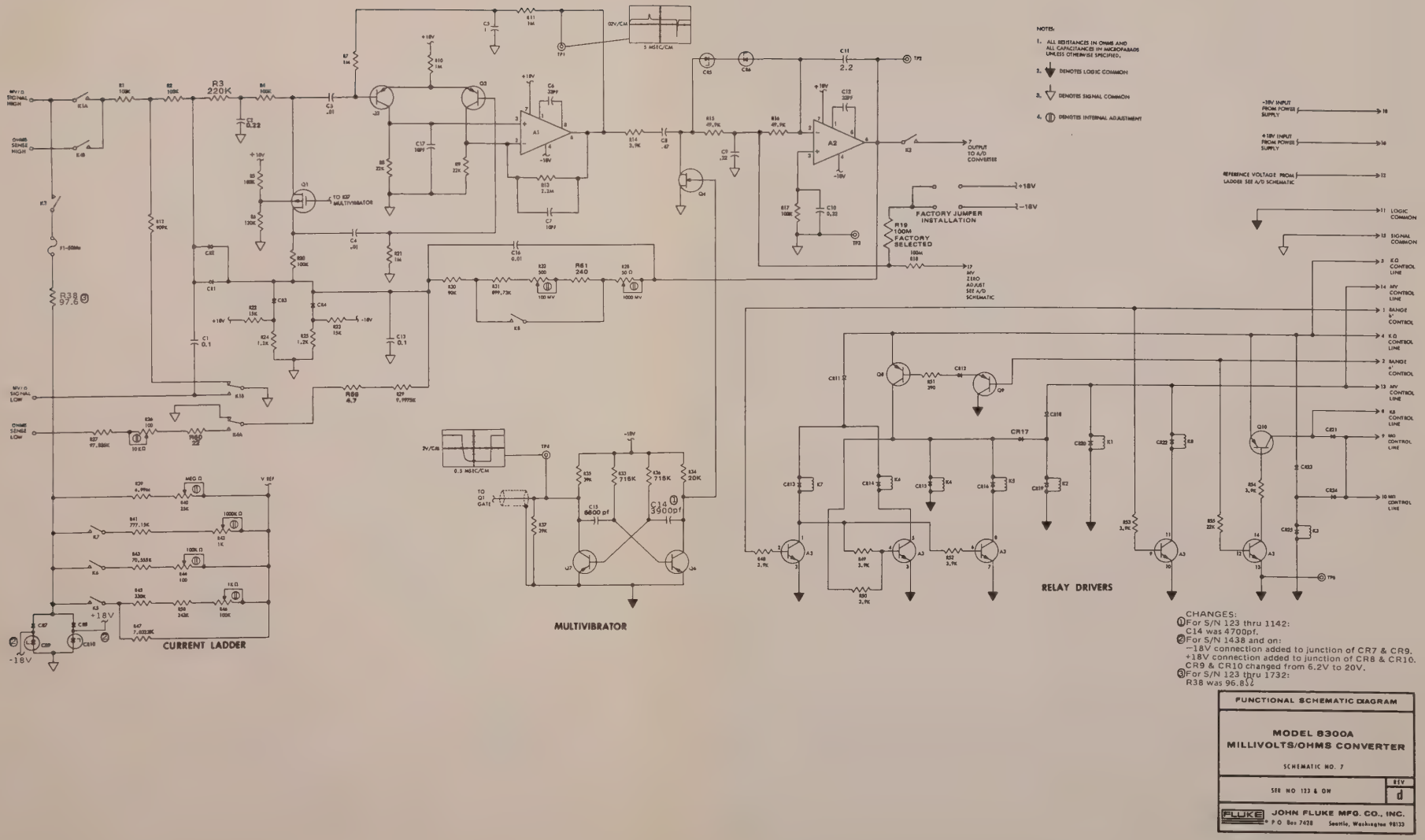


NOTE

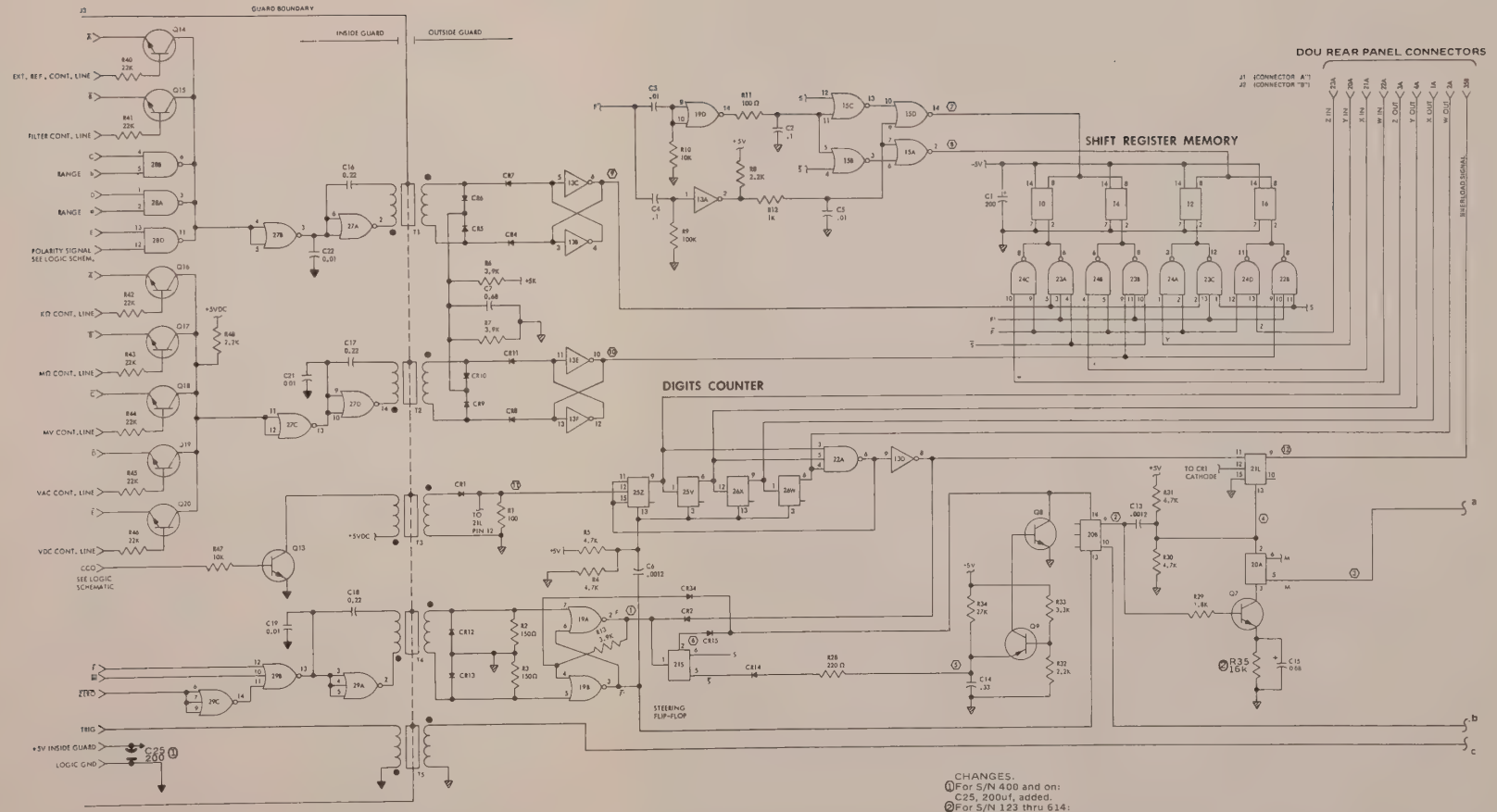
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. FLAGS OF LIKE NUMBER INDICATE MATCHED COMPONENTS.
3. DENOTES FRONT PANEL CONTROL
4. DENOTES INTERNAL ADJUSTMENT
5. DENOTES SIGNAL GROUND
6. DENOTES LOGIC GROUND

CHANGES:
① For S/N 123 thru 999: R12 was 16.2k

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A AC CONVERTER	
SCHEMATIC NO 6	
SER NO 123 & ON	REV d
JOHN FLUKE MFG. CO., INC. P.O. Box 7430 Seattle, Washington 98133	



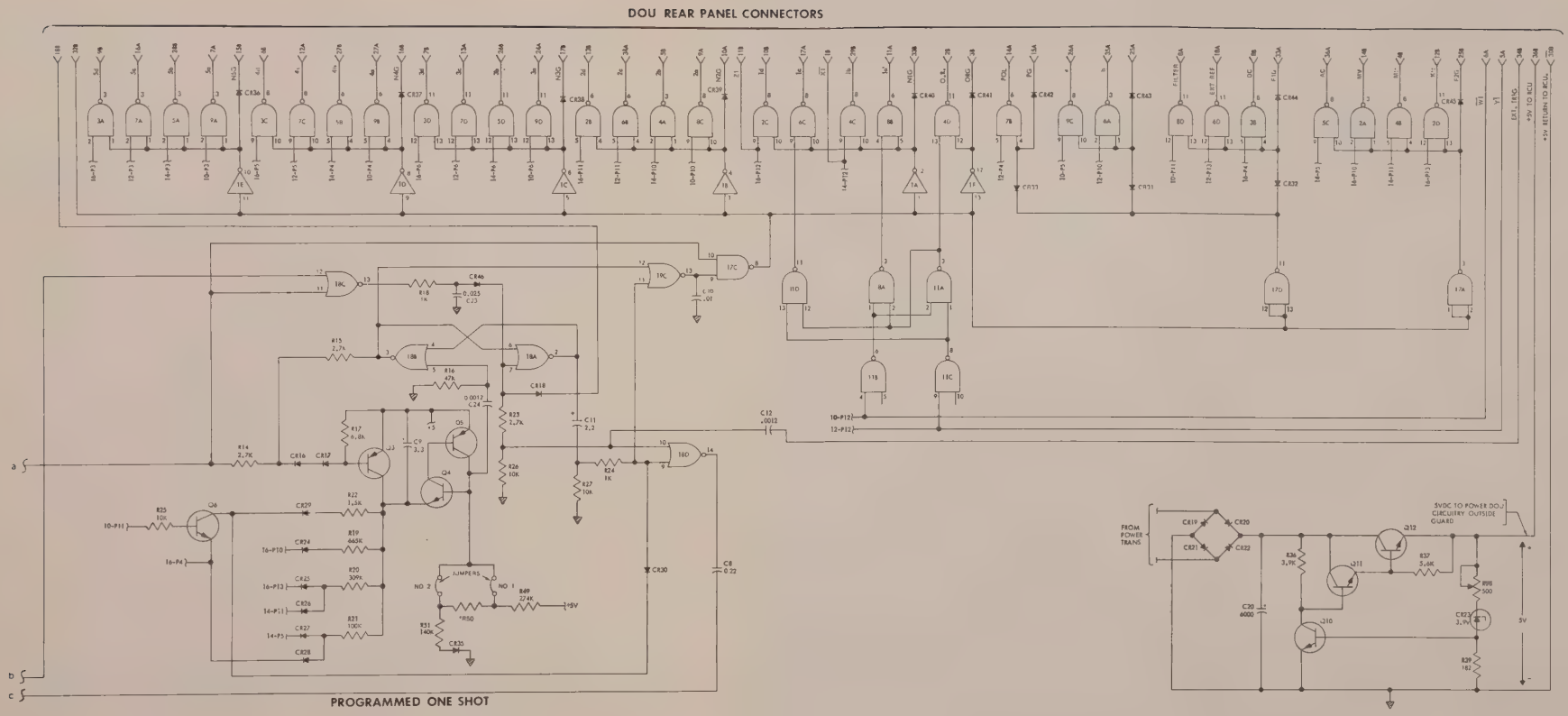
FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A MILLIVOLTS/OHMS CONVERTER	
SCHEMATIC NO. 7	
SER NO 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	



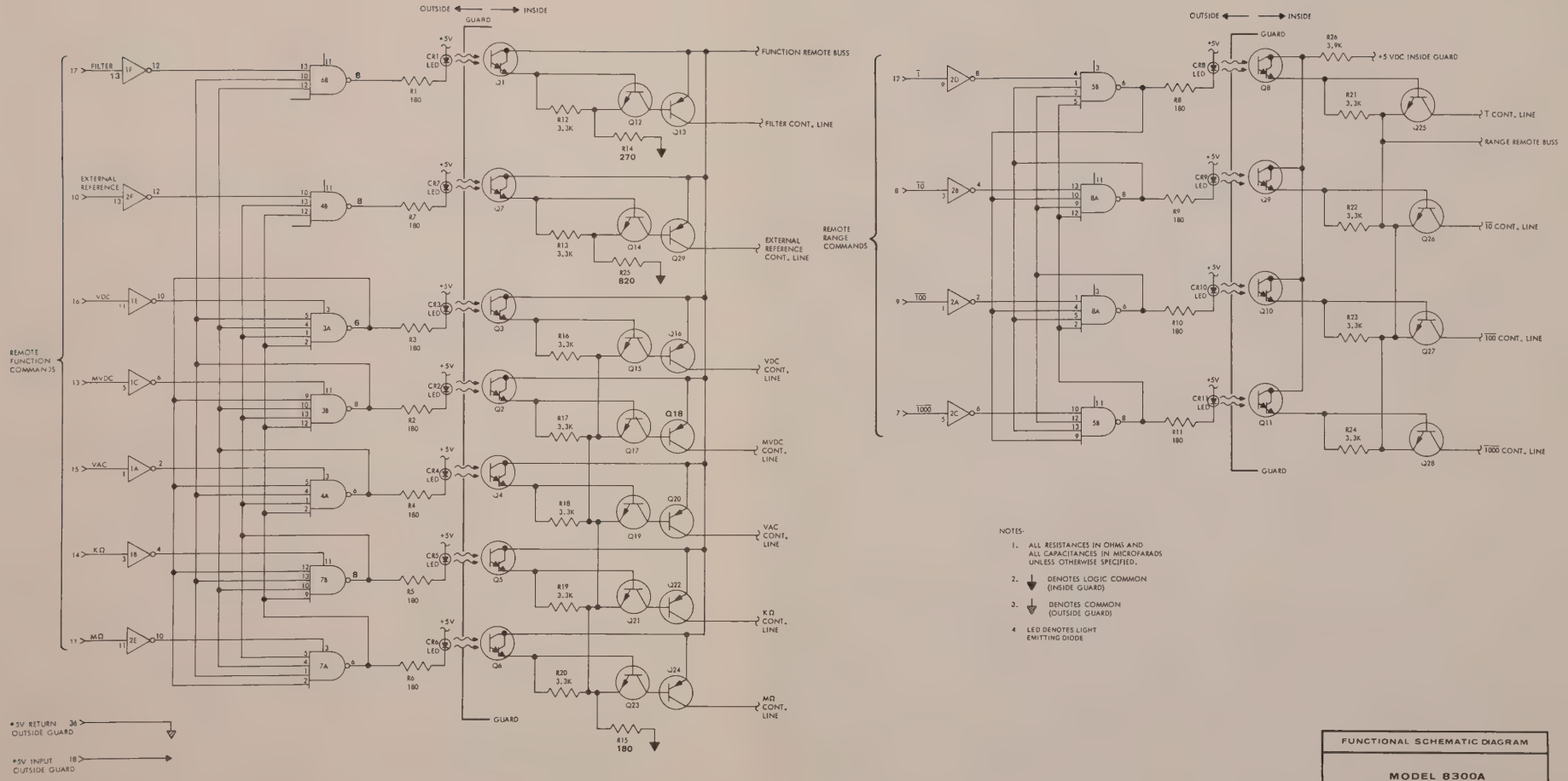
CHANGES.
(1) For S/N 400 and on:
C25, 200uf, added.
(2) For S/N 123 thru 614:
R35 was 15k.

NOTES:
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE NOTED.
2. ⏚ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ⏚ DENOTES COMMON (OUTSIDE GUARD)
4. * DENOTES SELECTED COMPONENT
5. ROUTING OF MEMORY OUTPUTS WITHIN THE DOU IS GIVEN BY NUMERICAL DESIGNATIONS. FOR EXAMPLE, "16–P3" REFERS TO PIN 3 OF SHIFT REGISTER 16.
6. ○ CORRESPONDS TO NUMBERED WAVEFORMS GIVEN IN FIGURES 6–4, DOU TIMING DIAGRAM.

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DATA OUTPUT UNIT	
SCHEMATIC NO. 8 SHEET 1	
SER NO 123 & ON	REV d
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



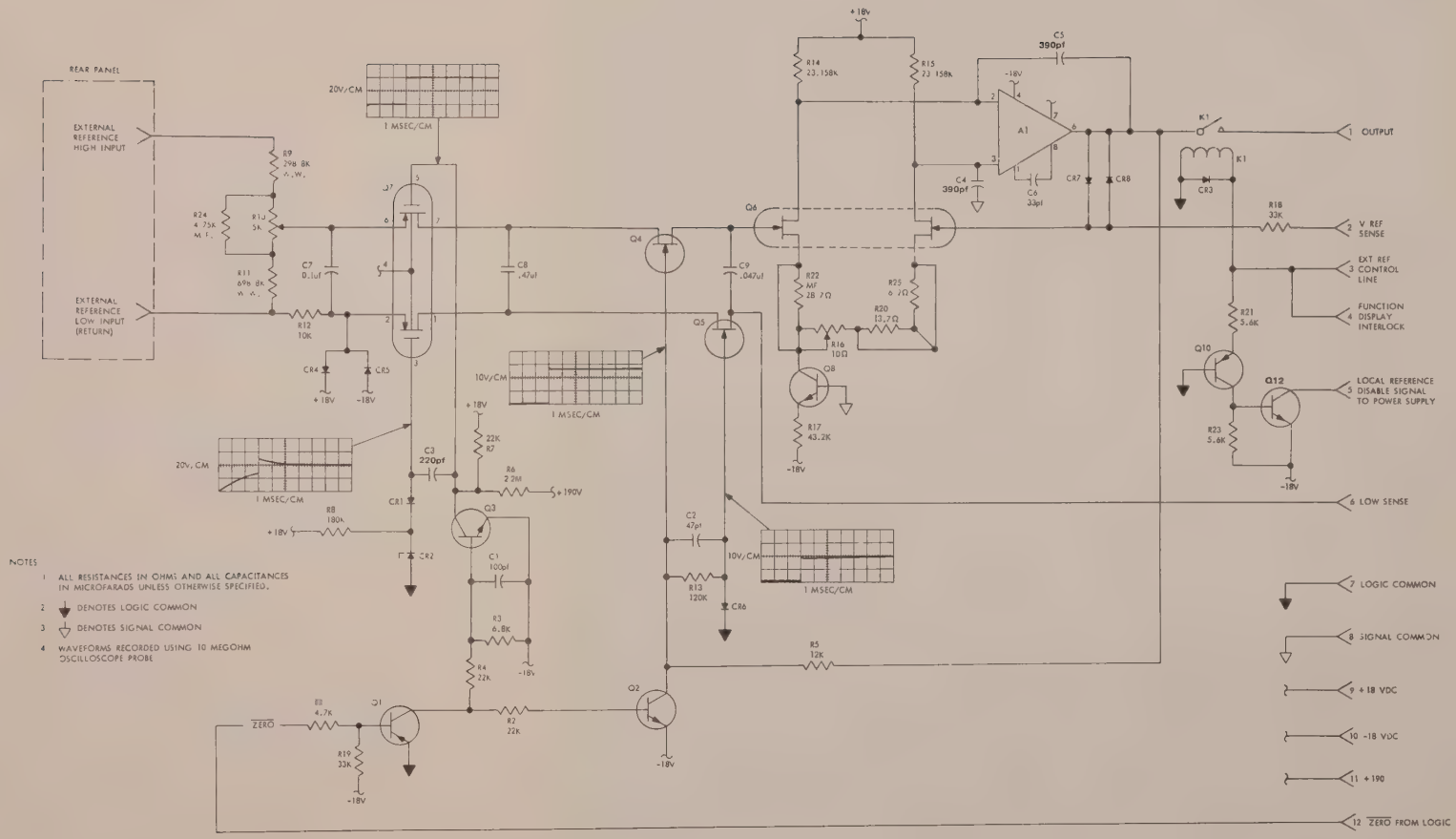
FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A DATA OUTPUT UNIT	
SCHEMATIC NO. 8 SHEET 2	
SER NO 123 & ON	REV C
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON (INSIDE GUARD)
3. ▽ DENOTES COMMON (OUTSIDE GUARD)
4. LED DENOTES LIGHT EMITTING DIODE

FUNCTIONAL SCHEMATIC DIAGRAM	
MODEL 8300A REMOTE CONTROL UNIT	
SCHEMATIC NO 9	
SER NO 173 & ON	REV B
FLUKE JOHN FLUKE MFG. CO., INC P O Box 7428 Seattle Washington 98133	



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⏚ DENOTES LOGIC COMMON
3. ⏚ DENOTES SIGNAL COMMON
4. WAVEFORMS RECORDED USING 10 MEGOHM OSCILLOSCOPE PROBE

FUNCTIONAL SCHEMATIC DIAGRAM

MODEL 8300A
DC EXTERNAL REFERENCE UNIT

SCHEMATIC NO 10

SER NO 123 & ON | REV C

FLUKE JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle Washington 98133

INTRODUCTION

The Model 8400A Digital Voltmeter is a five decade instrument with 20% over-ranging. Its main frame accepts a variety of analog and systems options that may be installed in the field at any time and in any sequence making it possible at any time to convert the instrument into a full system multimeter. Options include the AC Converter –01 Option, Resistance Converter –02 Option, Data Output Unit –03 Option, Remote Controlled Unit –04 Option, DC External Reference –05 Option, and AC External Reference –06 Option.

The 8400A uses the Recirculating Remainder analog to digital conversion technique which periodically samples the input and serially digitizes the sample providing a reliable DVM with a high long term accuracy and linearity, and outstanding environmental characteristics coupled with long term reliability.

BASIC 8400A

The basic 8400A measures DC voltages in five ranges with up to 1 microvolt of resolution and 20% over-ranging with an 1100 volt overload capacity. A non-blinking read-out contains an in line neon tube display showing polarity, over-range digit, and five full decades of digits. The speed at which the read-out updates, i.e. the input is sampled, is controllable by a variable Sample Rate Control available in both front panel adjustment and remote control operation. A switchable four pole filter has true broad band noise rejection that cannot integrate a constant offset error into the reading. The filter may be used with all analog options.

ANALOG OPTIONS

The AC Converter –01 Option makes it possible for the 8400A to measure AC voltages from 10 Hz to 100 kHz with up to 10 μV of resolution with a voltage limit of 1100 volts. A zero control is not needed to maintain the extremely low percent of range proportions of the specifications. The Resistance Converter –02 Option provides the instrument with seven resistance ranges from 10Ω to 10,000 KΩ making it possible to measure resistance up to 12 megohms. With the –02 resistance option installed, true four terminal measurements through the 10,000 KΩ range may be made. The DC External Reference Option provides four terminal DC to DC ratio measurements with ranges of $\pm$.01:1 to $\pm$100:1 while the AC External Reference Option provides three terminal AC to AC ratio measurements with reference ranges from 1 volt to 100 volts. Systems options such as the Isolated Remote Control and Isolated Data Output provide the instrument with complete systems interface capability.

BLOCK DIAGRAMS

BUFFER (A11) Figure No. 2

The Buffer, as shown in Block Diagram Figure 3, consists of an Input Divider which serves to attenuate the input. An Amplifier with a switchable gain for millivolt measurements followed by an Inverting Amplifier. It also contains the Logic circuitry required for Auto Ranging functions in the DC volts mode of operation.

The output voltage of the Buffer is zero to $\pm$10 volts inverted.

ACTIVE FILTER (A10) Figure No. 4

The Active Filter suppresses AC noise present in the Buffer output. It consists of a Voltage Follower and a Four Pole Filter. The filter may be selected by front panel or remote control. When filtering is not selected the circuit functions as a unity gain voltage follower. The output of the Active Filter is fed to the A-to-D Converter Assembly.

A-TO-D CONVERTER (A9) Figure No. 5

The A-to-D Converter consists of an Inverting Amplifier followed by a Polarity Detector and Switching system which feeds the A-to-D Amplifier. Display Storage, Sample and Hold, the Analog Comparator, the Ladders, and the Inverting Amplifier and Auto Zero Drive circuits are all located on this assembly.

The A-to-D Converter receives output from the Active Filter, detects the polarity, and switches the input FET's in such a manner as to always apply the input voltage to the amplifier in such a manner that its output is always positive. The output of the A-to-D Amplifier is connected to an Analog Comparator. The Analog Comparator produces current whenever the voltage out of the A-to-D Amplifier is above a predetermined level. It supplies its output current to the Constant Current Oscillator in the Logic Assembly.

Sample and Hold storage is included in the A-to-D Converter Assembly. Remainders of each digitizing period are stored alternately on the capacitors in Sample and Hold. When the instrument is in the Measurement Mode of operation, Display Storage stores analog values of digitized quantities in five separate capacitors. Display Storage consists of seven FET's connected in such a manner as to store these analog increments. Ladder Drivers cause the incremental switching in the Primary and Secondary Ladder circuits. The Primary Ladder feeds back to the input of the A-to-D Amplifier and the Secondary Ladder feeds the Display Storage through a monolithic amplifier.

LOGIC (A8) Figure No. 6

The Logic Control circuitry contains the Master Clock which produces 666 pulses per second which is coupled to a Six State Shift Register which generates the basic digitizing time periods. The Logic Assembly also contains the Current Controlled Oscillator which feeds the 16 State Binary Counter which translates the output of the Current Controlled Oscillator into BCD format. The Ladder Switches are also contained in the Logic Assembly.

Display Storage control pulses and the Analog Cycle Control pulses are generated in the Logic Assembly. These pulses control the various functions of the analog to digital conversion technique. The +7 Volts Reference Supply is also located on the Logic Assembly.

DISPLAY ASSEMBLY (A14) Figure No. 7

In addition to the seven gas filled display tubes and the Decoder Driver, the Display Assembly also contains the Anode Strobing circuitry used to display the digitized numbers in sequence as they are developed. Polarity Memory and Function Display are also contained in this assembly. The Sample Command Oscillator which controls the Measure and Storage time relationship is contained on this board, as is the Range Counter circuitry which provides the autoranging function throughout the instrument. Range and Function switches are also mounted on this assembly.

RANGE DELAY (A2) Figure No. 8

The Range Delay processes switching inputs from the front panel and produces control commands for the Range Decoder in the Display Assembly. It also produces UP and DOWN Autorange

commands for the Range Counter. The circuit consists of Logic, Range Delay 1 Shot, and a Pulse Generator. The Logic circuitry produces control signals for the Pulse Generator and the Decoder in the A14 Display Assembly. A clock signal for the Range Counter in the A14 Display is produced by the Pulse Generator. This clock signal is required for the Auto-range feature. The Range Delay 1 Shot produces a program time delay after any range change to allow for settling time of the analog signal conditioners which process the input.

POWER SUPPLY (A1) Figure No. 2

Four separate, but interdependent power supplies are contained in this assembly. A 200 volt Anode supply, +18 and −18 Operating supplies and a +5 volt Logic supply. The +5 volts is regulated by a reference voltage drop from the −18 volt supply.

CIRCUIT DESCRIPTIONS

BUFFER ASSEMBLY (A11) Drawing No. 8400A-1005

The Buffer consists of four basic elements. Input and Output voltage dividers, Amplifiers, and Control logic. The circuit has two operating configurations or modes as determined by the voltage selected, a low volts mode and a high volts mode. In the low volts mode, the 0.1 and 1.0 volt range, amplification of the input is required. In the high voltage modes, 100 and 1,000 volt ranges input attenuation occurs. In the 10 volt range, the input is processed without attenuation or amplification, since the output of the Buffer is zero to ±10 volts. The low volt input is applied across current limiting resistor R2, through the contacts of K1 to the high input impedance amplifier composed of three separate amplifiers - - a dual differential, operational amplifier composed of Q4 and Q5, U1, and an inverting amplifier U2. The output of the amplifier is applied in parallel to the A10 Active Filter and to a gain determining output voltage divider R37 through R40, through contacts of relays K1 and K6. In the low volt mode of operation voltage follower U3 is used to boot strap the operational environment of the input dual differential pair Q4 and Q5 with the input voltage to increase its effective ratio of common mode rejection. Offset voltage present that would cause Buffer output with no input, is compensated for by use of two potentiometers, one a coarse DC ZERO which balances the basic meter voltages of the input to the differential amplifier Q5 by adjusting the collector current ratio; and the second potentiometer Buffer ZERO which affords a fine adjustment, by applying just that amount of known voltage to the base of differential amplifier Q5B, that results in a Buffer output voltage equal to zero when the input voltage is zero. Buffer ZERO, which is the fine adjustment, is available via a front panel access.

Overload protection for the dual differential amplifier is afforded by CR1, R2, Q11, and the current limiting resistors previously defined as R1 and R2 shown on the wiring diagram. Positive overload protection is afforded by transister Q11 which clamps the amplifier output to 1.7 volts. Negative over-voltage protection is afforded by diode CR1 which clamps the input to −1.7 volts. The current drawn during an overload is limited by the total input resistance of 147 K ohms.

Compensation circuits have been provided to reduce the temperature coefficient of the input offset voltage and offset current. Transistor Q2 and the surrounding circuitry, R18 and R19, provides the temperature variable base current required by input transistor Q5. Transistor Q3 compensates the temperature variation of the basic meter voltage in dual transistor Q4 to insure that the input transistor Q5 remains at substantially the same bias condition, irrespective of temperature.

ACTIVE FILTER (A10) Drawing No. 8400A-1015

The Active Filter as shown in schematic drawing number 8400A-1015 consists of a voltage follower proceeded by four poles of low pass filtering. These poles attenuate undesirable AC signals which

may be present on the DC input signal. Filtering occurs after the FILT switch has been depressed or filtering called for by the remote controlled unit when the instrument is in a systems application. A block diagram of the active filter is shown in Figure 4. An Active Filter is used for better response time.

A-to-D CONVERTER (A9) Drawing No. 8400A-1003

Inverting Amplifier

Input from the Active Filter is fed to the Inverting Amplifier whose output is connected to the Polarity Detector and to the minus input to the A-to-D Amplifier. The Polarity Detector detects the polarity and switches Q7 or Q8 in such a fashion as to always place a positive voltage on the input of Q20. When the input is positive, FET Q8 turns ON and applies a positive input to transistor Q20. Conversely, when the input to the instrument is negative, Q10 senses the negative voltage and switches Q7 which takes the positive output out of the Inverting Amplifier and applies the positive output to the input of Q20. Thus, input to the A-to-D Amplifier is always positive on the "A" side of Q20. An Automatic ZERO drive circuit consisting of transistors Q5, Q6, and capacitor C2 has been included. The Auto ZERO signal also drives transistor Q3 to turn OFF, thereby removing input to the Inverting Amplifier during the ZERO Offset correction time period. The GATE 4 signal is applied to the emitters of Q10 and Q11 in the Polarity Detector, enabling the Polarity Detector only during the "A" digitizing period when the instrument is in Measurement Mode. During the remainder of measurement period the plus and minus gates Q7 and Q8 are turned OFF and polarity information is retained by the display circuit, Polarity Memory.

A-to-D Amplifier

The A-to-D Amplifier consists of dual FET Q20 and monolithic amplifier U2 and the associated components. The offset removal circuit is composed of transistors Q23, Q24, and capacitor C7. Switch Q24 is turned ON during the ZERO time period when the instrument is in Measurement Mode. This signal also controls switches Q19 and Q31 which are turned ON during the ZERO time period. Q30 which is turned OFF during the ZERO time period to disconnect the Amplifier output from the Ladder. Transistor Q29 and resistor R54 constitute a clamp which prevents the A-to-D Amplifier from saturating when its output is above 7 volts.

Analog Comparator (A9)

The Analog Comparator consisting of Q32, Q33, Q34, and Q35 is a voltage comparator. Differential amplifier Q35 compares the A-to-D Amplifier output with a +7 reference and Q33, Q34 outputs the resultant current to the Current Control Oscillator. Transistor Q32 operates as a second comparator which responds quickly to high voltage levels, thereby allowing maximum time for the resolution of the last pulse.

The Sample and Hold circuit consists of transistors Q25 through Q28, and capacitors C9 and C10. The sequence of operation is as follows: C9 stores the first remainder, C10 stores the second remainder, C9 the third remainder, C10 the fourth remainder, C9 the fifth remainder. The remainders are alternately stored and released by the action of the FET switches Q25 through Q28 and the gate pulses GATE 2, GATE 1-22 and GATE 11.

Ladders

The Ladders are controlled by the Ladder Switches Q37 through Q44 which are driven by the Ladder Drivers located on the Logic Assembly (A8). The output of the Ladder Switches is

applied to two Ladders simultaneously. Each Ladder comprises a four-bit weight resistor digital to analog converter. The Primary Ladder consists of resistors R44 through R50 and produces an output that corresponds to the actual value of the digital input. The Secondary Ladder which drives only the display storage circuits through Buffer Amplifier U3, consists of resistors R40 through R43 and produces an analog value that is proportional to the digit that has been digitized in each period. A half digit bias is produced by R38 and R39 in conjunction with the Secondary Ladder's resistors and adds the voltage equivalent of half a digit to the output of the Secondary Ladder. This insures proper display storage by compensating for the effects of any possible voltage decay in the storage circuit.

Display Storage

The Display Storage circuit consists of FET switches Q13 through Q37, capacitors C11 through C15, and FET switches Q12 and Q18. The buffered output of the Secondary Ladder is supplied to the appropriate storage capacitor through Q18, which is enabled during the second half of each digitizing period. The first and most significant digit is stored on C13 and the least significant digit is stored as a charge on C14. These capacitors receive their analog charge in Measurement Mode as each digit is initially digitized. Q12, the output FET, is not enabled until Storage Mode and then places the output of each capacitor on the input of the A-to-D Amplifier and as each analog value is redigitized, during the last half of each time period, that digit is replaced as an analog charge in its respective capacitor by the action of Q18. Thus, the same reading is continually digitized and displayed until a new sample is taken.

LOGIC (A8) Drawing No. 8400A-1004

The Logic Assembly contains a Master Clock and a Shift Register that generate and divide to produce the timing functions for the instrument. In addition, it contains the Constant Current Oscillator and Binary Counter plus the 7 Volt Reference Supply.

Master Clock

The 333 Hz clock signal is produced by transistor Q1. The clock frequency is determined by the RC time constant of resistor R1 and capacitor C1. The output of the Clock is applied to the clock input of flip-flop U1B. The Q output of U1B is inverted by Q4 and becomes the $\overline{H}$ signal.

Shift Register

The 6 State Shift Register consists of 5 J-K flip-flops U3A, U3B, U4A, and U1A. U2B is used to generate the $\overline{ZERO}$ pulse which is the first timing period of each cycle of the instrument. When the NAND gate U2B receives all high signals from the $\overline{A}$ through $\overline{E}$ lines it produces a $\overline{ZERO}$ pulse. The Q outputs of the Shift Register supply the A through E digitizing period pulses. Outputs from the 6 State Shift Register are also fed to Display Storage Control which generates the storage pulses used in display storage in the A-to-D Converter Assembly.

Constant Current Oscillator

The Constant Current Oscillator consisting of a multivibrator Q1 and Q3 generates a pulse train whenever it is supplied current by the Analog Comparitor. The pulse train is fed to a 16 State Binary Counter. The binary output of that counter is fed to the Ladder Switches and to the Decoder Driver in the Display Assembly. The truth table for the 16 State Binary

Counter is shown in Figure 13. Directly below the 16 State Binary Counter are shown four transistors Q19 through Q22 which are the Ladder Switches and are connected to the Ladder Drivers located on the A-to-D Assembly.

Analog Cycle Control

The Analog Cycle Control consisting of Q11 through Q17 and accepts various basic time pulses and generates the special pulses such as the GATE pulses, STORE IN and STORE OUT pulses.

+7 Volt Reference Supply

The 7 Volt Reference for the instrument is derived by using a Reference Amplifier, U9, which also encompasses a zener diode reference. Amplifier U10 and emitter follower Q25 are connected as an operational amplifier which presents a low source impedance at the reference point. Transistor Q24 disables the 7 Volt Reference in the event the user wishes to employ an external reference when the required options are installed. Transistor Q23 coupled with the zener diode in the Reference Amplifier produce the +7 Volt Reference.

DISPLAY (A14) Drawing No. 8400A-1002, Sht. 1 and Sht. 2

The BCD input from the Counter is coupled to Decoder Driver U4. U4 translates the BCD count into a low signal on the appropriate decimal line to the display tubes. Each display tube is pulsed ON in sequence with its respective digitizing period by the pulse appearing at the bases of Q22 through Q26 which are enabled by the $\overline{F}$ pulse appearing at Q34 which means that the display tube can ionize only during the last half of each of the digitizing periods. A11 through Q18 serve to light the decimal points in the Display Assembly by the action of the signals coupled to their emitters and bases. Polarity Memory circuit receives its information from the Polarity Detector. Once having been pulsed, the flip-flop will turn to the appropriate state so that when the C pulse enables the base of Q9 and Q10, whichever is conducting, it can place a low on the appropriate sign in V1.

Sample Command Oscillator

The Sample Command Oscillator consists of a programmable unijunction transistor, Q8, and the surrounding circuitry. Resistors R12 and R14 provide a bias level for the gate of the Programmable Unijunction Transistor (PUT). C3 charges through R16 and R17 and when the PUT conducts, capacitor C3 is discharged. This generates an output pulse which commands the Measure/Store cycle J-K flip-flop U3A located adjacent to the Range Counter flip-flop. U3A generates the M and $\overline{M}$ pulses which control the Measure time. Varying R16 in the Sample Command Oscillator will vary the sample rate of the instrument. The ZERO pulse fed to the clock input of U3A insures starting the Measure Mode at the beginning of a timing cycle.

If the instrument is ranging, SIGNAL 3 entering the junction of R9 and CR7 in the Sample Command Oscillator will disable Q6 which in turn disables the Sample Command Oscillator to allow time for the analog signal conditioners to settle on the new range before a new Measurement Mode is entered.

When SAMPLE RATE control is switched to the external position and sampling is initiated through the EXTernal trigger, input of the Data Output Unit Option will cause a near ground potential to appear on the emitter of Q6. Its collector follows causing the gate of Q8 to be more than .6 volts below the anode and the Programmable Unijunction Transistor fires once. If the corresponding sample rate results in a range change, the Range Delay One-Shot Multivibrator will disable the Sample Command Oscillator via SIGNAL 3 entering through CR7. This means that Measurement Mode may not be commanded until the Range Delay One-Shot times out. At the end of this time delay the Sample Command Oscillator is automatically retriggered via CR8 and SIGNAL 2 from the Range Delay One-Shot. Diode CR9 and resistor R10 insure that capacitor C3 will rapidly charge to be ready for the next trigger pulse. SIGNAL 8 interrupts the Cycle Control Shift Register on the logic assembly (A8) by forcing it directly to the "E" digitizing period. This is done to minimize the time between the Sample Command to start a Measure Mode and the actual start of that Measure Mode.

Over Range Driver

The Over Range Driver is a means of detecting a maximum count of 12 during the first time period when the instrument is in its highest possible range. This is done through the action of Q3, Q4, and Q5. Q3 has coupled to its base the Constant Current Oscillator output pulses, to its emitter the $\overline{UP}$ pulse. The $\overline{UP}$ occurs on the eleventh count in the "A" time period and goes low enabling transistor Q3. At the next CCO pulse, which would be the twelfth pulse, transistor Q3 will conduct enabling Q5 and placing the 5 volts on DS5 in the function display assembly which will turn on the OVER lamp.

Q4 is a monostable device and requires resetting once it goes into conduction, which is accomplished by the following Measure pulse coupled through C1 which differentiates the signal and resets Q4 turning OFF the OVER lamp. When the Over Range Driver is in its conducting state it produces from the emitter of Q37 a SIGNAL 7 which is used in the Range Delay Assembly to stop the Range Oscillator preventing the instrument from trying to seek a higher range. Q2 located above the Over Range Assembly has no application in the Over Range function. It is used to accept the filter signal which turns on the Input Filter in the instrument causing Q2 to cut off and cause an additional delay in the Range Delay Multivibrator so when filter is selected the Ranging Oscillator is operating at a lower frequency in order to compensate for the additional settling time required in the instrument.

Range Counter

The Range Counter is composed of three J-K flip-flops. Flip-flop U3B has a clocked input that is SIGNAL 6. This signal originates in the Range Oscillator and is pulsed with each firing of the Range Oscillator. The Range Counter is a divide by 6 counter that provides 6 possible binary states for range counting. Five pulses being considered an UP range command and one pulse being considered a DOWN range command. Signal 6 applied to the clock input of the range flip-flop U3B alters the 6 state of the Range Counter. Transistor Q35 is provided to reset U2B which may be in an unallowed state as a result of initial instrument turn ON. The output of U3B is fed back to the clock inputs of U2A and U2B providing their input for a proper Range Code advancement.

RANGE DELAY (A2) Drawing No. 8400A-1006

The Range Delay Assembly consists of Gate, a Range Delay One-Shot Multivibrator, and a Range Oscillator. The gates allow the specified set of ranges to be obtained which is dependent upon the function called. The Range Oscillator generates pulses which trigger the Range Delay One-Shot while simultaneously causing the Range Counter to change states. The Range Delay One-Shot prevents further ranging for a specified time to allow the analog signal conditioners to settle in the new range. This time is variable depending upon whether Filter has been selected or not.

The gates are U2A, U2B, U2C, U3A, and U3B. Gate U2C and U3A are UP range stops. Gate U2C prevents autoranging above the 10,000 range while gate U3A prevents autoranging above the 1,000 range in the VDC function. Gates 2A and 2B are DOWN range stops. Gate U2A prevents autoranging below the 10 range in the ohms function while gate U2B prevents autoranging below 0.1 in any function. Gate U3B is the master UP range control and enables the Range Oscillator only if an UP range is expected.

The three inverters U1D, U1E, and U1F coupled with the UP range enable line provide one input for UP range control gate U3B. The result is that U3B is enabled for 1.5 milliseconds or the second half of the "A" digitizing period of Measurement Mode if an UP range is to be executed.

Signals applied to diodes CR6, CR7, CR8, and CR10 coupled with the range DOWN enable line provide a negative going signal to the range oscillator at the end of the "A" digitizing period in a Measurement Mode if a DOWN range is to be executed.

Range Oscillator

The Range Oscillator is composed of capacitor C4 and resistors R14 and R18 and transistor Q4. The output of this oscillator appears at the cathode of Q4. Q4 is fired discharging capacitor C4 through R15 when the gate is about −.6 volts relative to the anode. Thus, Q4 is fired to produce one output pulse by lowering its gate voltage or by raising its anode voltage such that the voltage difference between these elements is .6 volts. The firing of Q4 discharges capacitor C4 and reduces the anode and gate voltages. Thus, Q3 will turn on and force the anode and gate of Q4 to the same potential. Q4 turns off and capacitor C4 charges through R14 and R15. If the firing potential between the gate and anode of Q4 is established, Q4 fires again and the cycle is repeated to produce the second output pulse. The frequency of oscillations is set by the level of gate voltage applied and the charging time constant of R4, R18, and capacitor C4.

Control of the gate of Q4 is affected by two mutually exclusive inputs. One of these associated with the ranging UP and the other associated with ranging DOWN. In an UP range situation, the output of U3B goes low for about 1.5 milliseconds during which time the Range Oscillator outputs 5 pulses. In a DOWN range situation, the DOWN range enable line goes low. This This signal is capacitively coupled by C3 to the gate of Q4 causing it to output one pulse. Five pulses counted by the Range Counter, located on the Display Assembly, commands a transition to the next higher range, while one pulse commands a transition to the next lower range. In either case, the first output pulse triggers the Range Delay One-Shot to allow the analog signal conditioners to settle in the new range.

Range Delay One-Shot Multivibrator

Transistors Q1 and Q2 make up the Range Delay One-Shot Multivibrator. A range change pulse from the Range Oscillator turns transistor Q2 ON and turns transistor Q1 OFF, placing

the One-Shot Multivibrator into its unstable state. The RC charge time of combined capacitors C2 and C6 and resistor R5 determine how long the One-Shot remains in its unstable state. With the filter selected, no current flows through R16 and the time out is about 220 milliseconds. When the filter is not selected, the time out is decreased to about 25 milliseconds because of the additional current path offered through R16 as a result of the SIGNAL 4 line potential which is established in the Display Assembly. The SIGNAL 3 line disables the Sample Command Oscillator during range delay time and SIGNAL 2 retriggers the Sample Command Oscillator at the end of the range delay time.

POWER SUPPLY (A1) Drawing No. 8400A-1100

The Power Supply consists of four regulating circuits supplying +18 and −18 volt operating supplies, a 200 volt supply for display tube ionization, and a 5 volt logic supply.

The +18 and −18 volt operating supplies are operated from the full-wave rectifiers consisting of diodes CR5 through CR8 and filter capacitors C2 and C5. The +18 volt regulator consists of operational amplifier U1 and series pass transistor Q3. The voltage reference for the +18 volt operating supply regulator is derived from reference amplifier U9 and a temperature compensation transistor located on the Logic assembly. The −18 volts is referenced to zener diode CR9.

The +200 volts regulator is operated from a full-wave rectifier and filter consisting of diodes CR1 through CR4 and capacitor C1. The reference for the +200 volts regulator is furnished by the +18 volt supply. Voltage variations are amplified in transistor Q2 and applied to the series pass transistor Q1.

The +5 volt regulator is operated from a full-wave rectifier and filter consisting of CR10 through CR13 and capacitor C8. The reference for the +5 volts regulator is taken from the −18 volts via a voltage divider formed by R14, R15, and R17. The series pass element is a compound emitter follower composed of transistor Q8 driving power transistor Q6. Voltage variations which are detected by the sample string R14, R15, and R17 are amplified by Q7.

AC CONVERTER −01 OPTION Drawing No. 8400A-1007

Operational Rectifier

Input FET Q1 functions as a source follower while transistor Q2 provides a low impedance guard voltage which is used to boot-strap most of the capacity that otherwise would appear between the gate and the circuit common. The first two differential pairs are in a dual in-line package U1, and together with Q4 and Q5 develop the required gain. Transistors Q3 and Q6 function as current sources with values such that clipping due to overload is symmetrical. Changes in capaciter charges are small and amplifier recovery time is minimized. Transistor Q7 compensates for capacitance losses in the diodes.

DC Difference Amplifier/Integrator

The filter network which provides the input to the Amplifier/Integrator consists of a multi-section RC filter matched in such a manner as to maintain a good Common Mode Rejection. Gain for the DC amplifier is provided by a monolithic operational amplifier U2 with a total open-loop gain of approximately 5 times 10^5.

Range and Function Control

The converter input and output relays K1 and K2 are operated from the VAC control lines. The range relays K4 through K6 are operated by driver circuitry consisting of NAND gates U4A, U4C, and U4D. These range control gates accept the Buffer output of the range counter. U3B and U4B deliver the UP and DOWN range stop commands for VAC function through the range delay assembly. The NAND gates U3A and U3C deliver the set and reset commands to the Range Counter for prevention of illegal or disallowed ranges in the volt AC function.

OHMS CONVERTER –02 OPTION Drawing No. 8400A-1010

The Ohms Converter is operated in one of two configurations associated with the functions of Ohms and Kilohms. In the Ohms function, the convertor is a constant current source which is connected to the terminals on the front panel of the 8400A. In KΩ function the Ohms Converter is the precision scaling resistor, which, in conjunction with the Buffer Amplifier located in the basic instrument, and the unknown resistor produces a voltage proportional to the unknown resistance.

Constant Current Generator

Regulated DC voltage is developed by resistors R2, R4, R5, zener diode CR3, Transistor Q1, and operational amplifier U1. The divider string R6, R7, and R8 scales the zener reference voltage and applies it to amplifier U2. Range resistors R10 through R16, in conjunction with zener CR3, apply a range dependent constant current to the emitter of Darlington pair composed of Q2 and Q3. Fuse F1 capacitor C6 and diodes CR2 and CR4 are used as an overvoltage protection circuit for the current generator.

Range Scaling Network

Resistors R17 through R22 and relay contacts K1A, K2A, and K4 are the Range-Scaling Network. Relay contacts K1A and K2A are actuated by range selection. Relay K4 is actuated in the KΩ function and connects one end of the scaling network to the high source terminal on the front panel.

Relay Drive Circuit

Range control relay K1 receives its call commands from the Buffer Assembly, whereas K2 receives its call commands from the Range Counter. Function control relays K3 and K4 are controlled by transistors Q5 and Q6. Our manual range condition is detected by gate U5E which enables gates U5C and U5D to control Q5 and Q6. In an autorange condition, gates U5C and U5D are disabled and function control is transferred by gate U3B to RS flip-flop U3A and U3C. Mutually exclusive outputs of this flip-flop in turn control switches Q5 and Q6. Gates U4A and U4B operate on the set and reset lines of the RS flip-flop to enable an automatic change of function in an autorange condition.

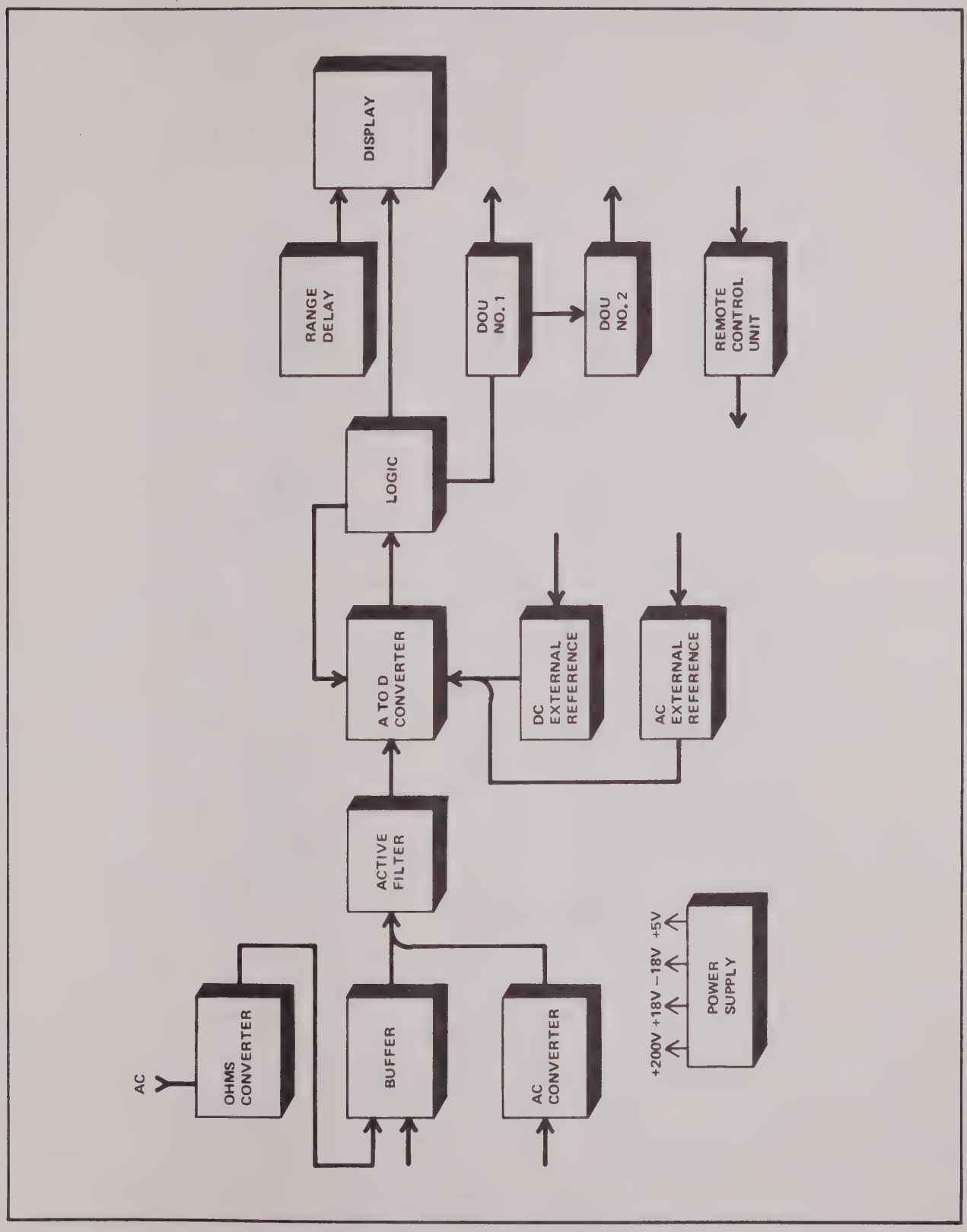


FIGURE 1. MODEL 8400A BLOCK DIAGRAM

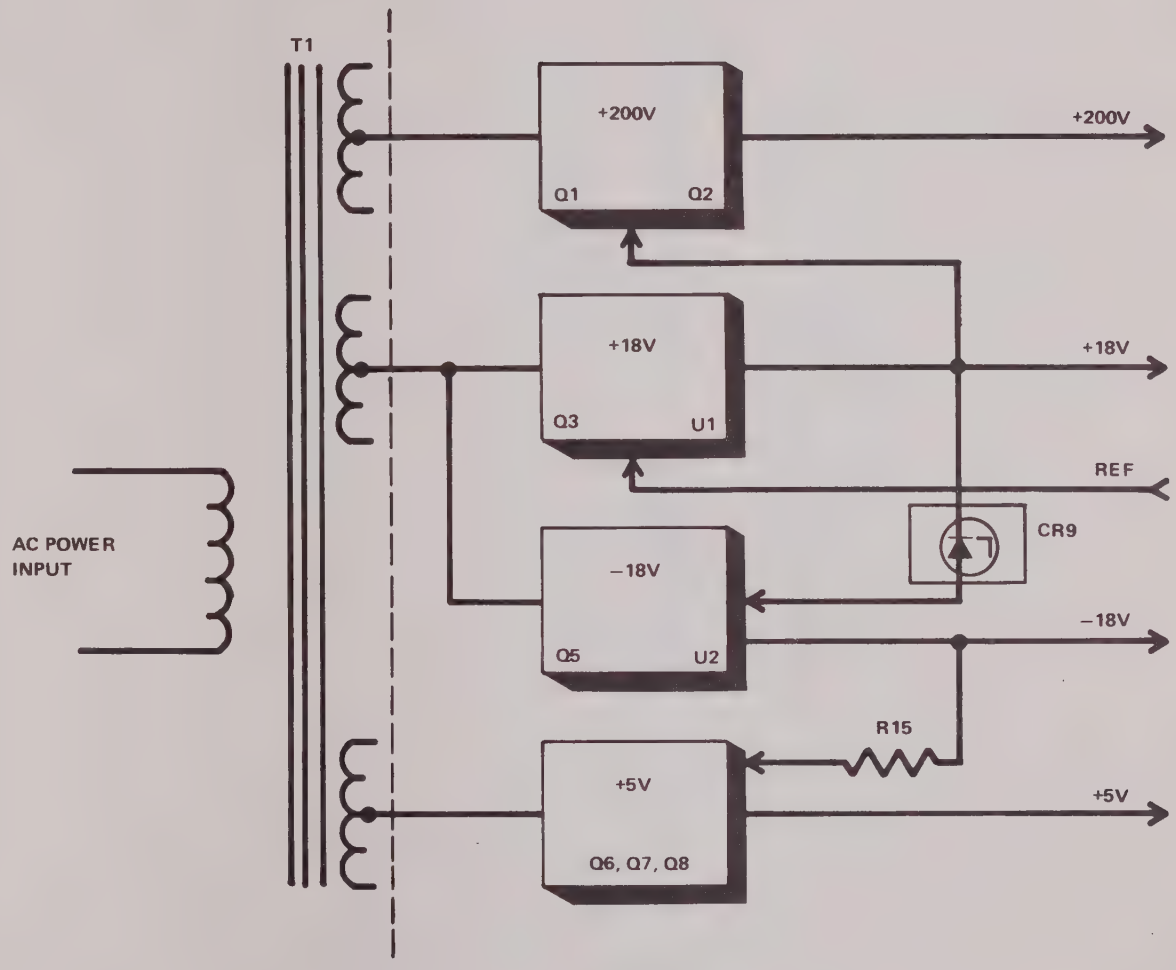


FIGURE 2. A1 POWER SUPPLY

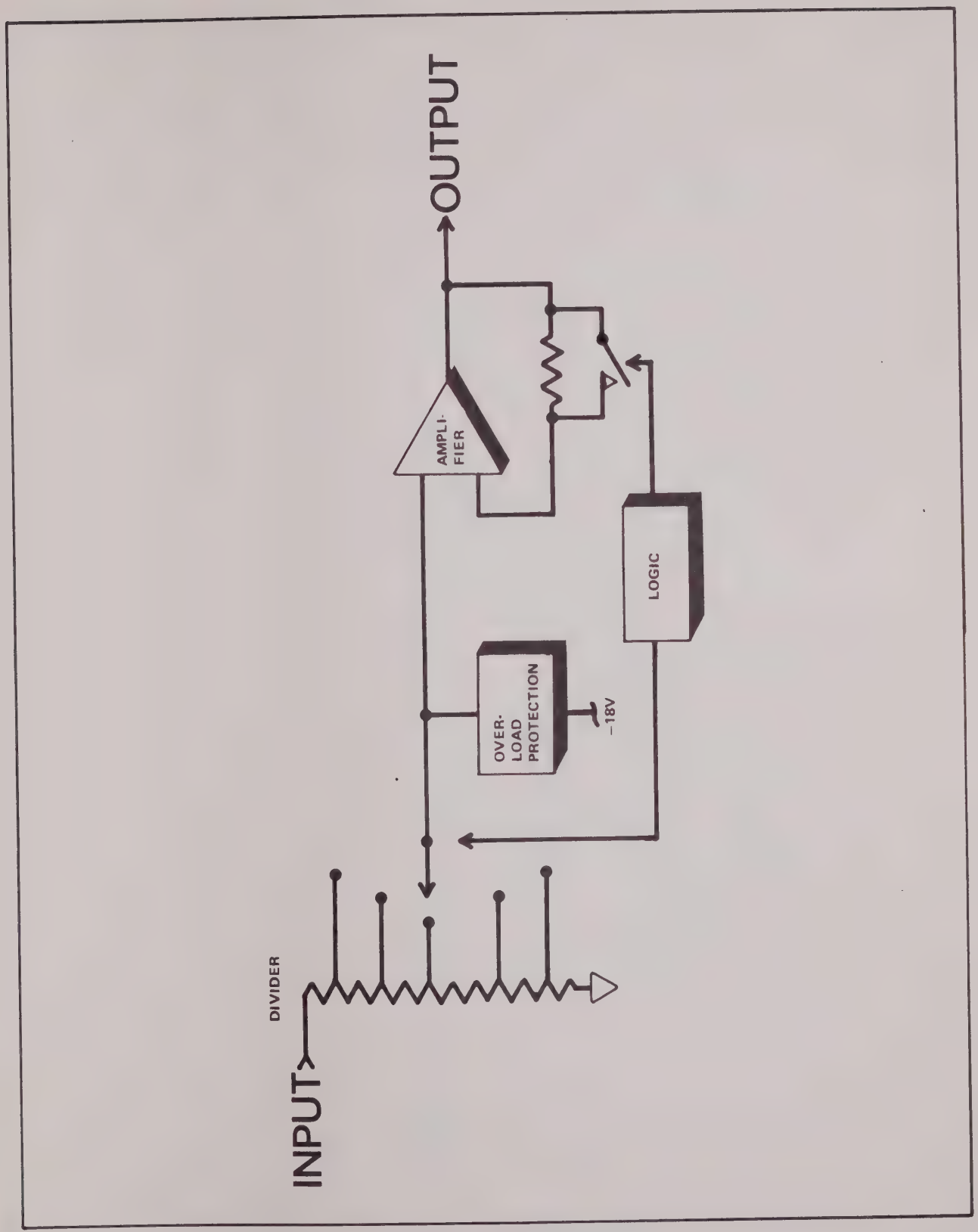


FIGURE 3. A11 BUFFER

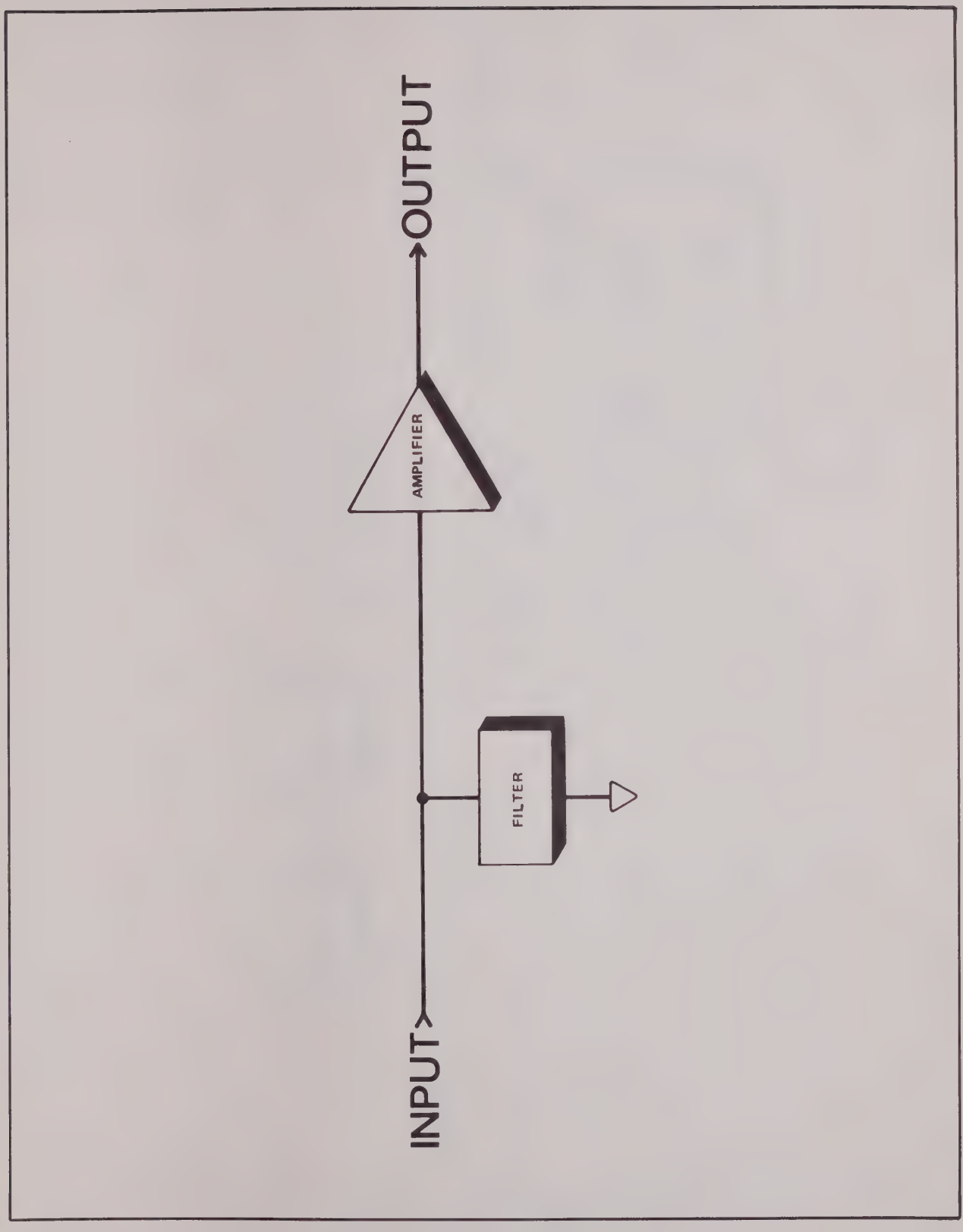


FIGURE 4. A10 ACTIVE FILTER

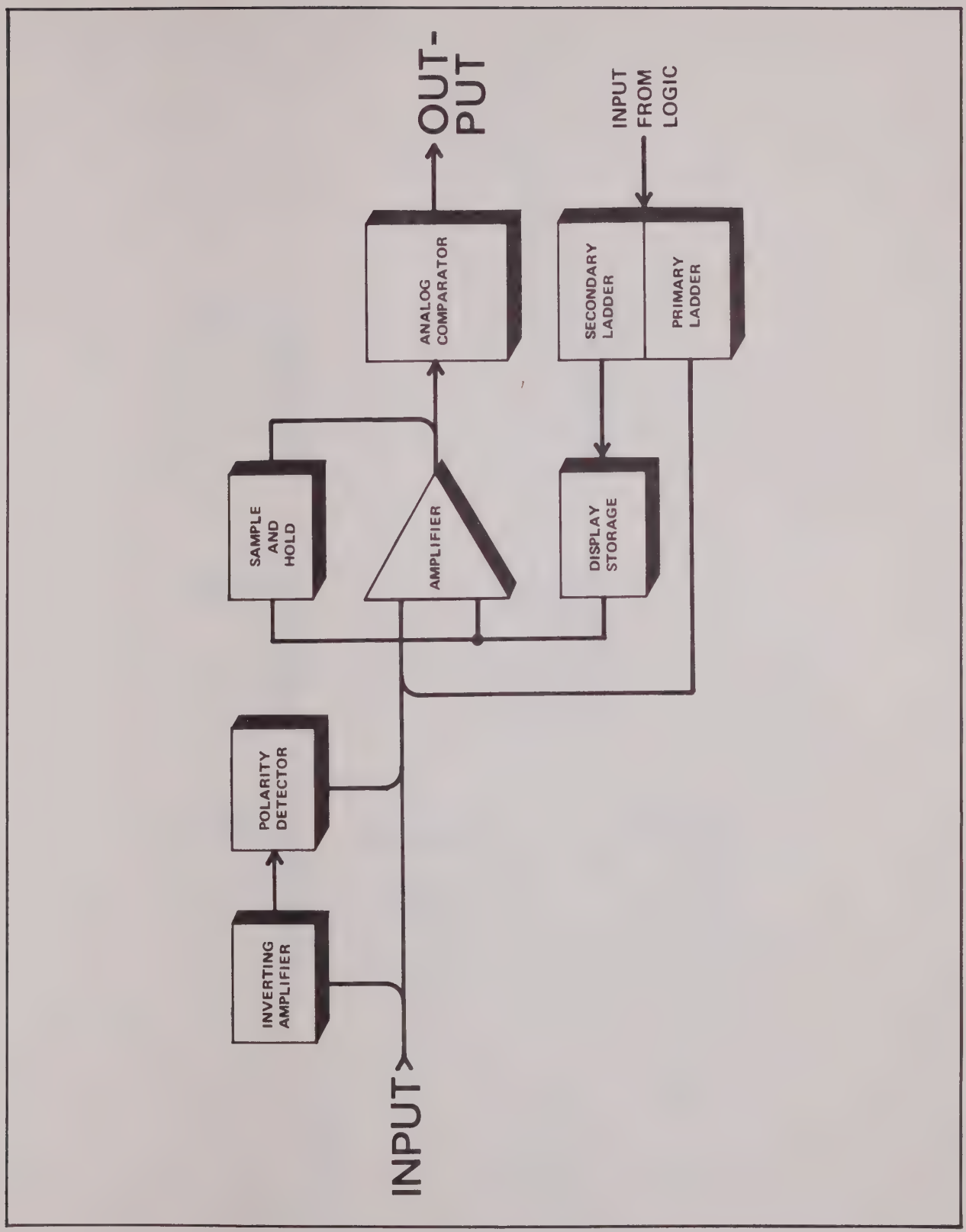


FIGURE 5. A9 A-TO-D CONVERTER

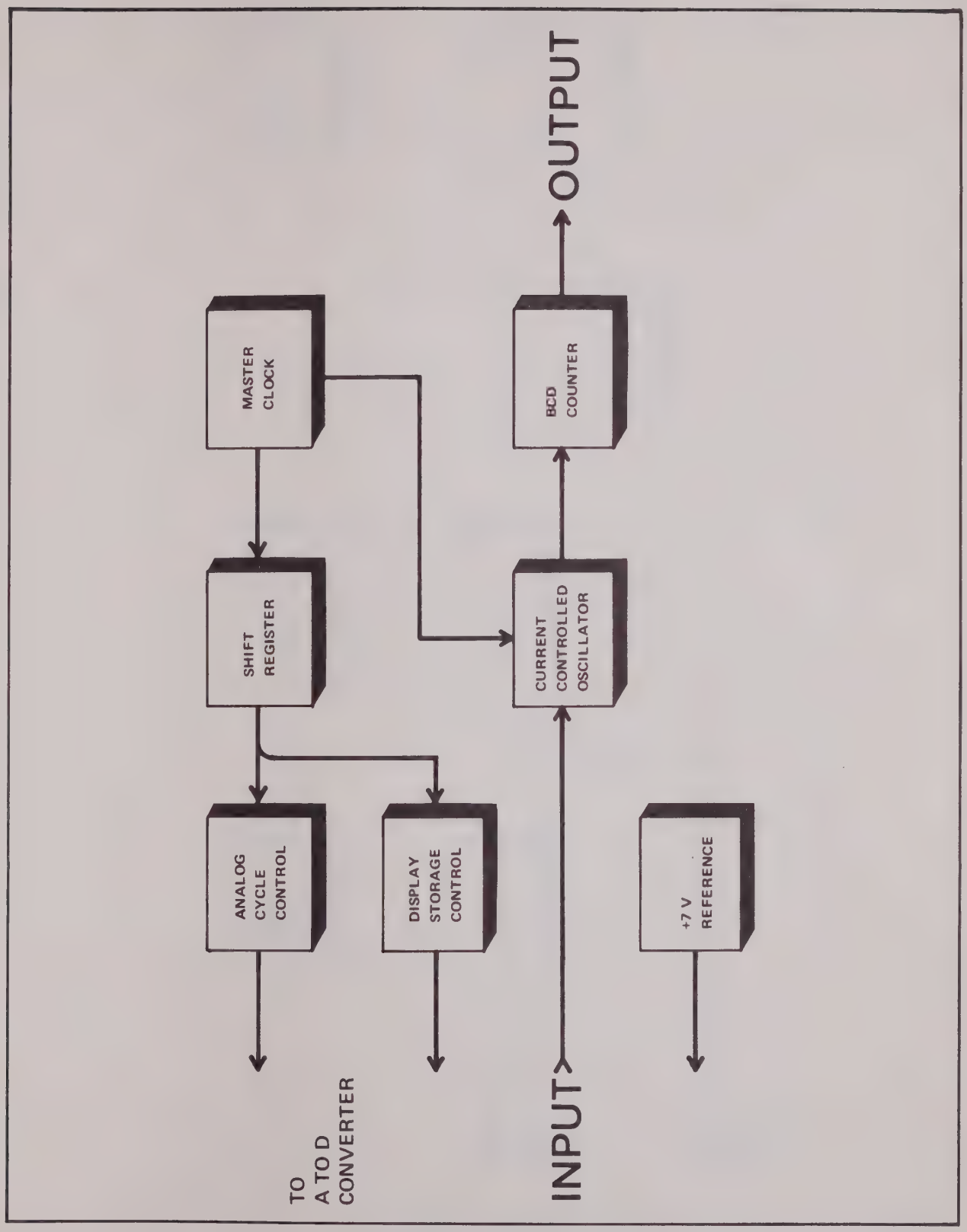


FIGURE 6. A8 LOGIC

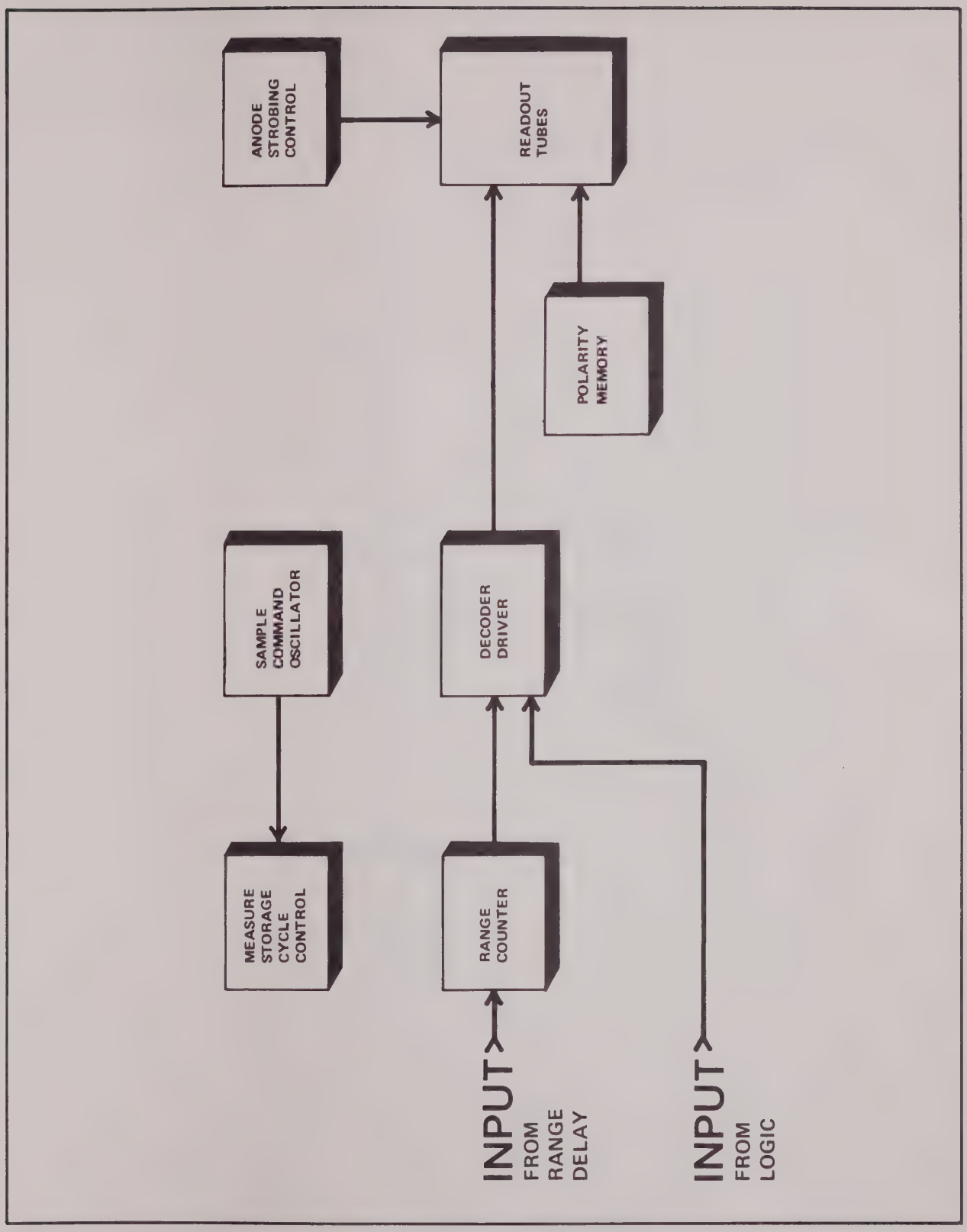


FIGURE 7. A14 DISPLAY

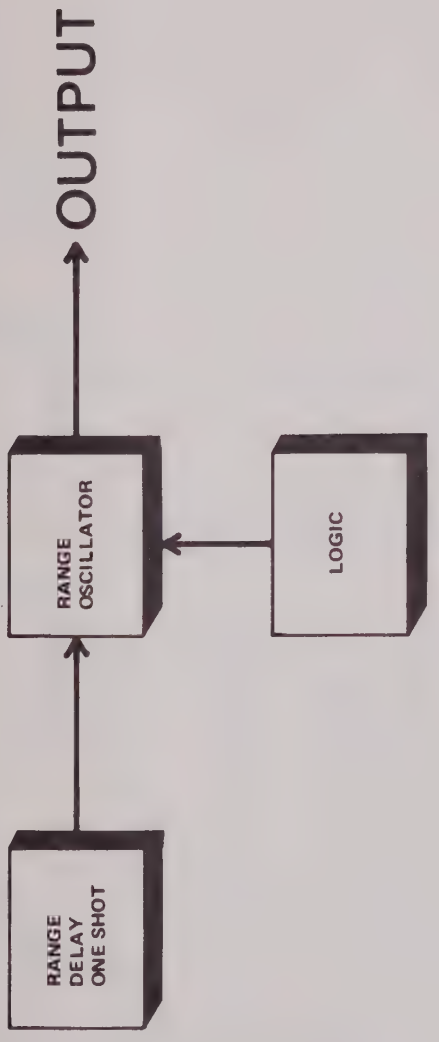


FIGURE 8. A2 RANGE DELAY

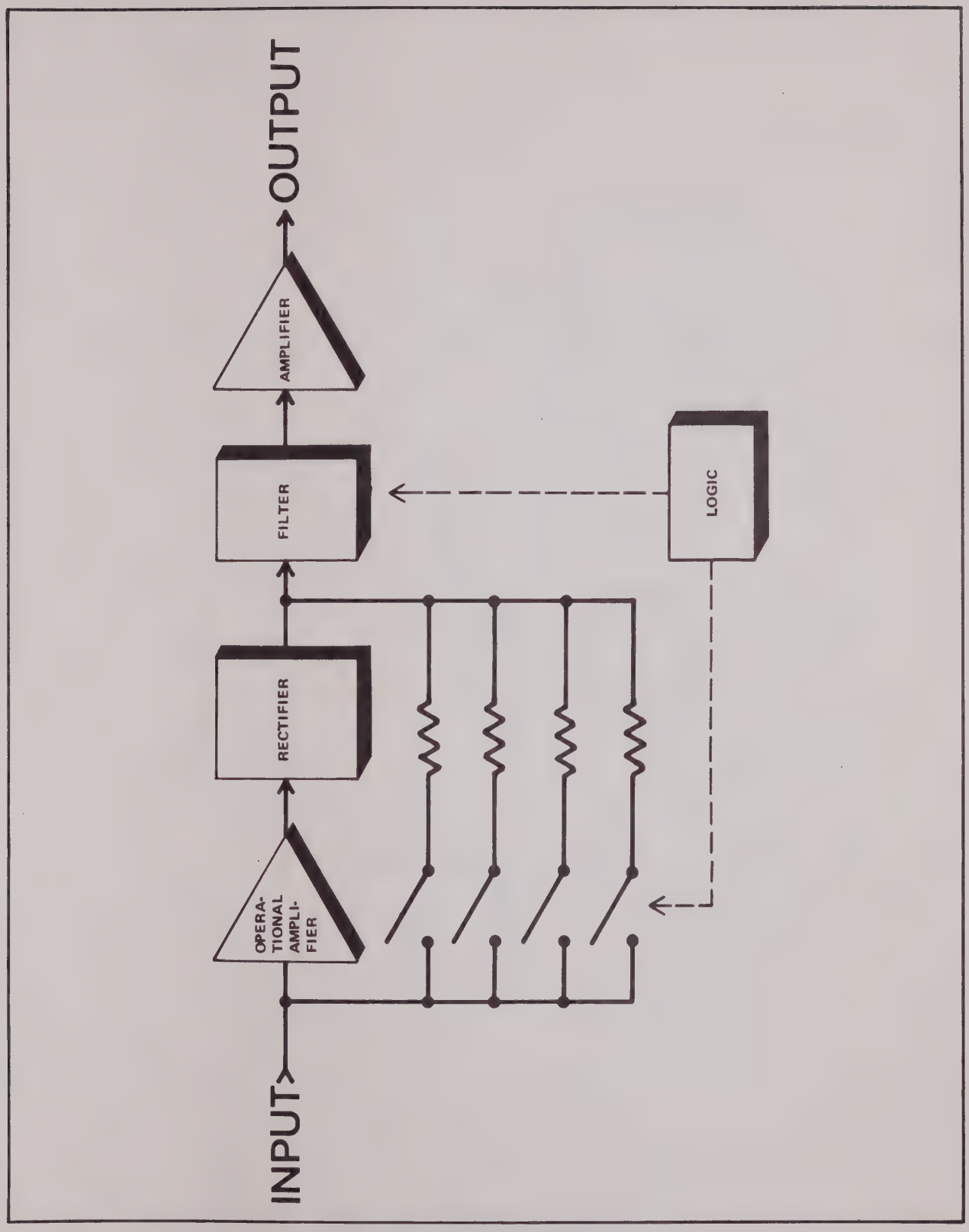


FIGURE 9. A13 AC CONVERTER

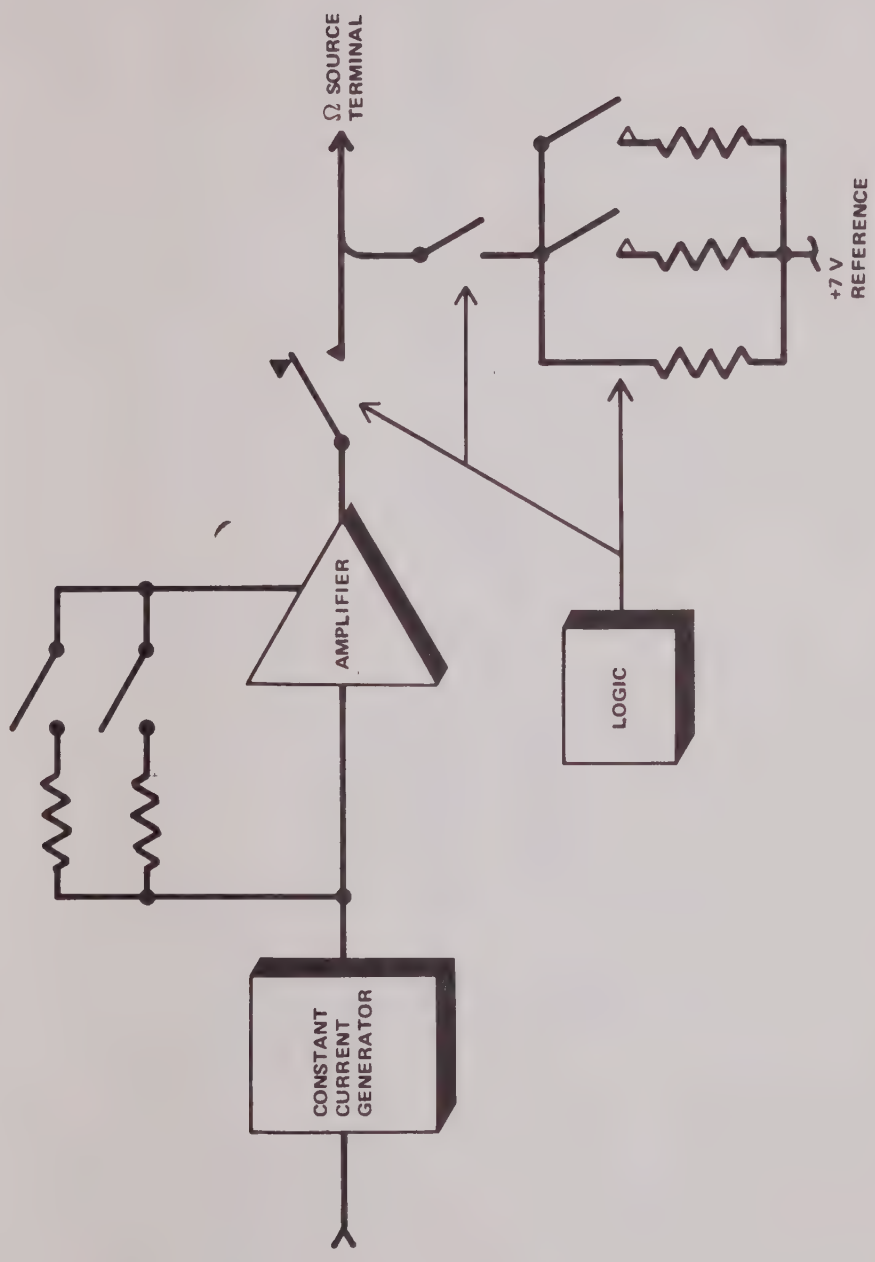


FIGURE 10. A12 OHMS CONVERTER

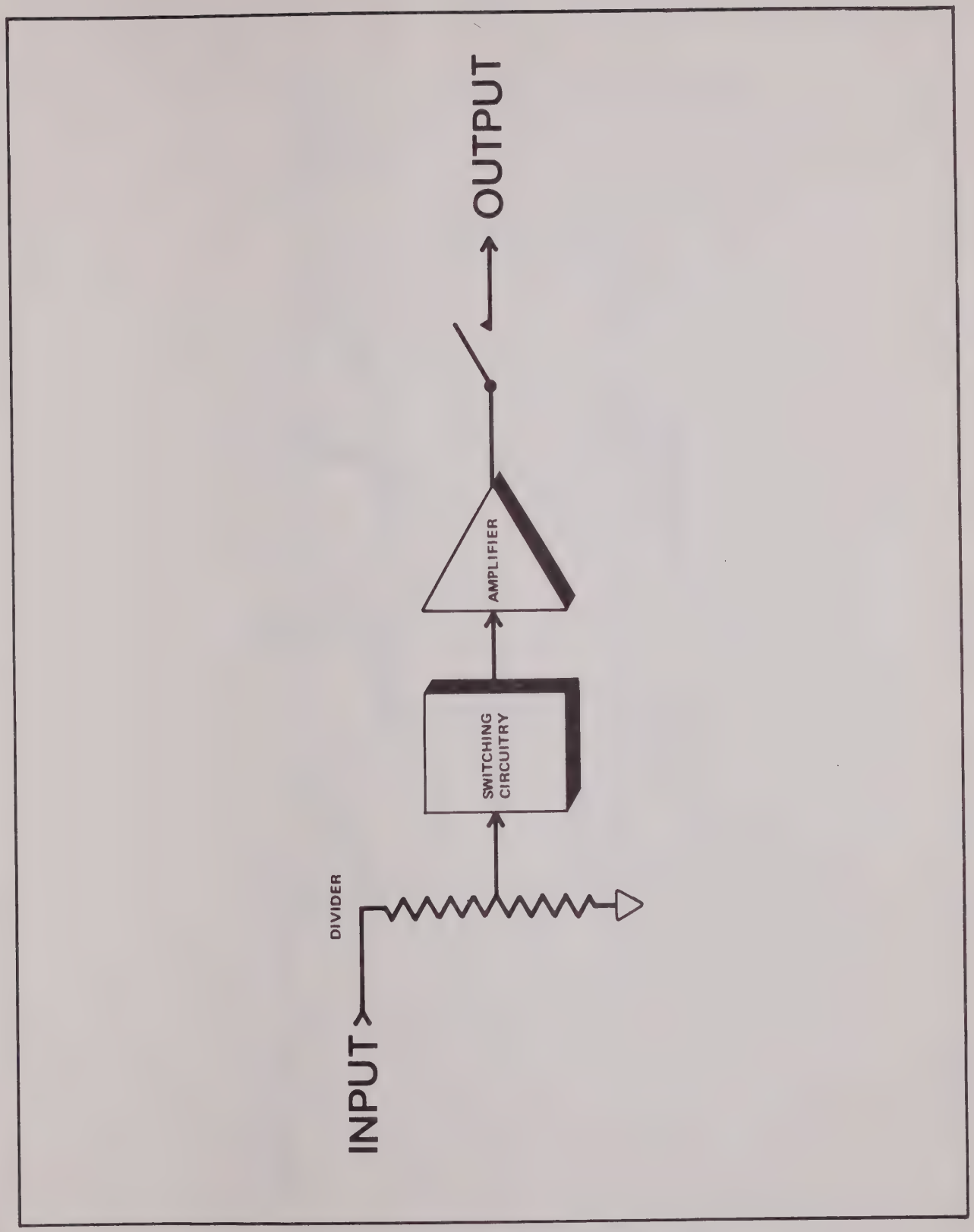


FIGURE 11. A3 DC EXTERNAL REFERENCE

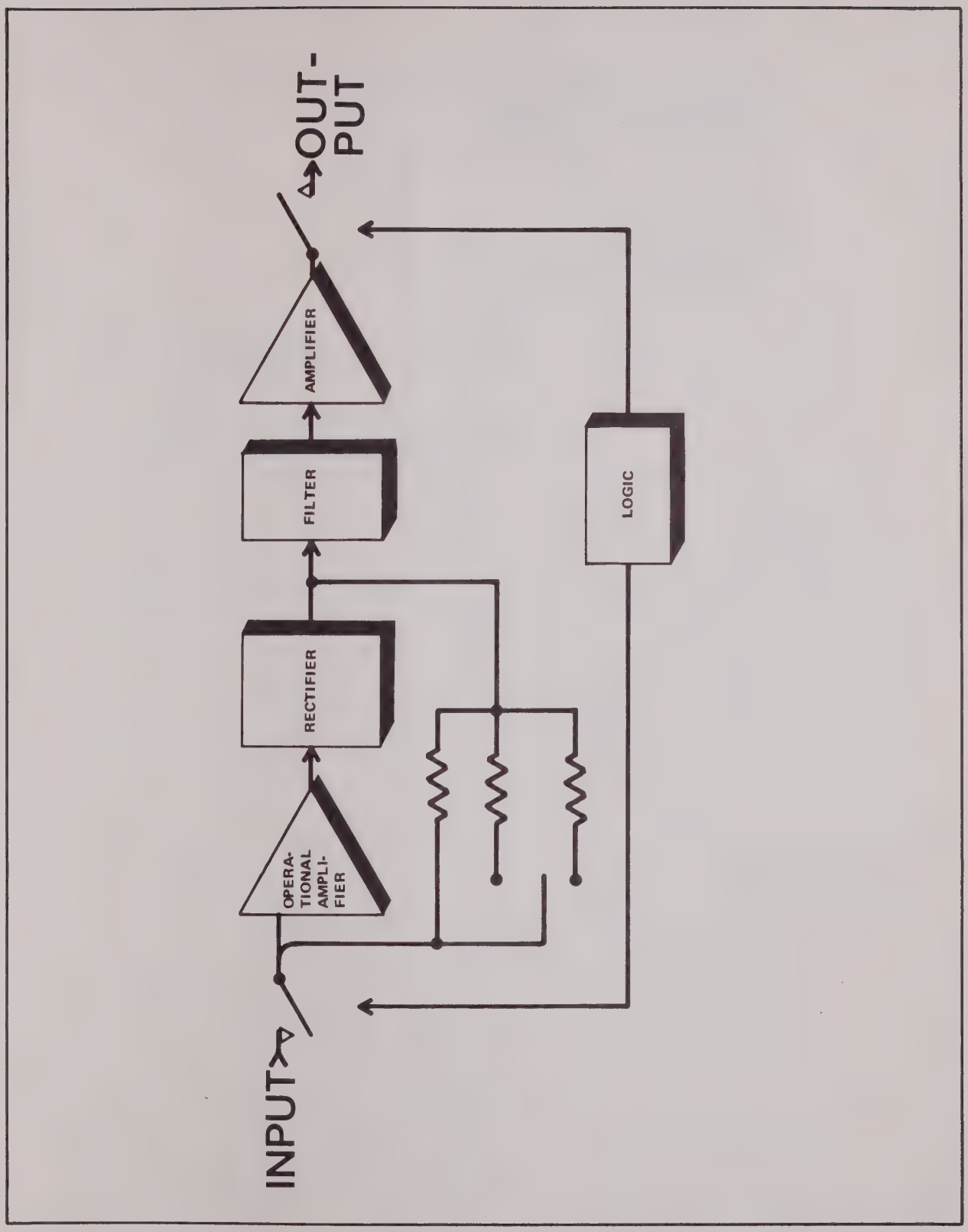
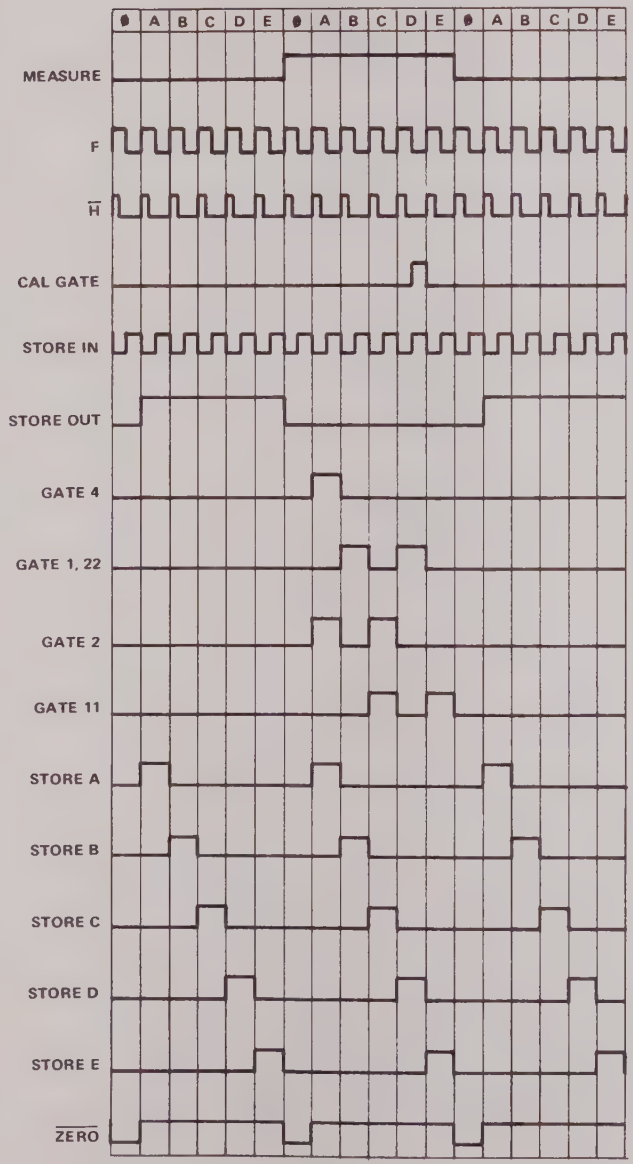


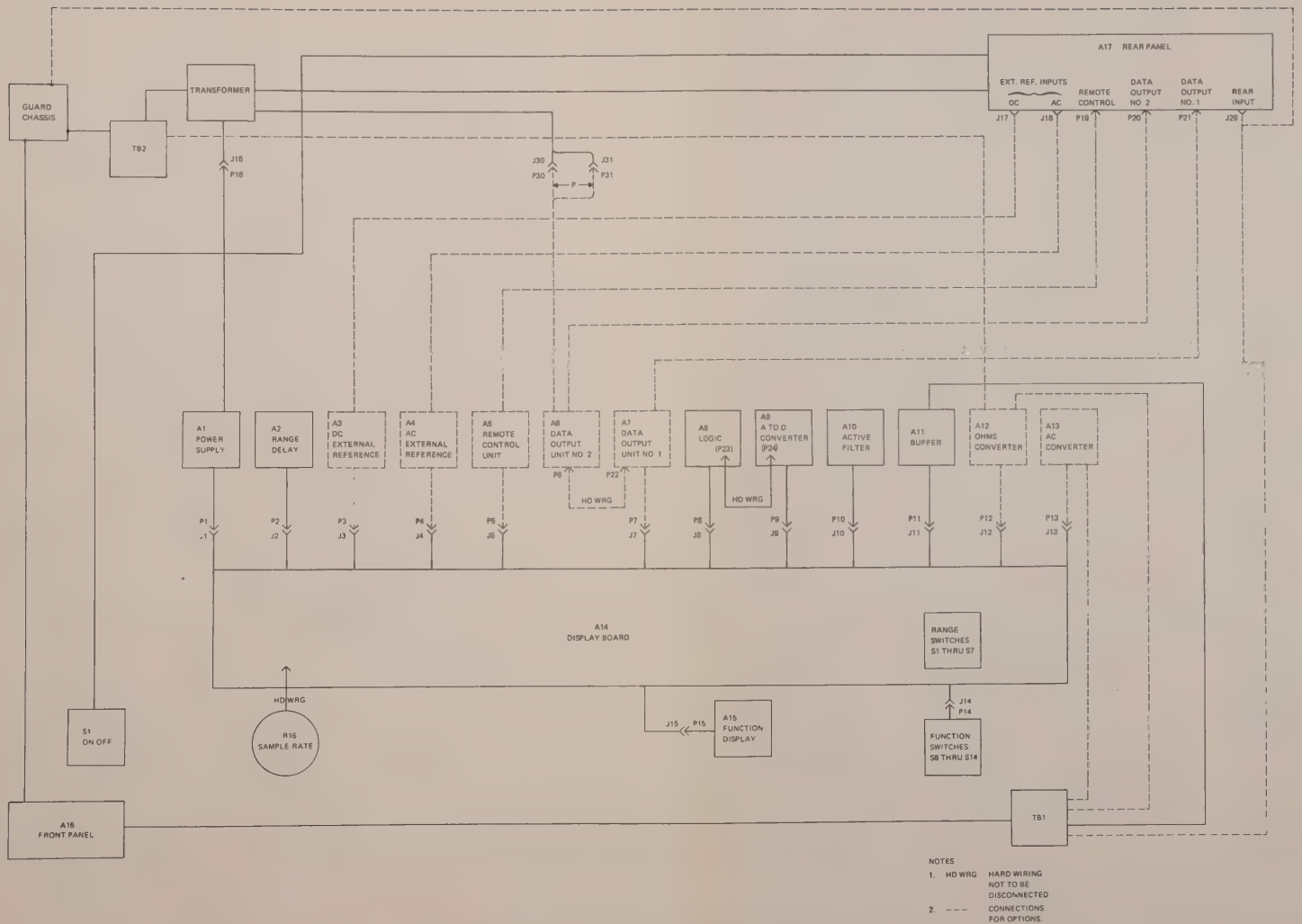
FIGURE 12. A4 AC EXTERNAL REFERENCE

SUBPERIOD	SHIFT REGISTER FLIP FLOP AND ZERO GATE OUTPUT STATES					
	U3B	U3A	U4A	U4B	U1A	U2B
ZERO	0	0	0	0	0	0
A	1	0	0	0	0	1
B	0	1	0	0	0	1
C	0	0	1	0	0	1
D	0	0	0	1	0	1
E	0	0	0	1	1	1



CCO PULSE COUNT	SIXTEEN - STATE BINARY COUNTER			
	U5B Z	U5A Y	U6A X	U6B W
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

FIGURE 13. COUNTING CIRCUIT



NOTES

1. HD WRG — HARD WIRING NOT TO BE DISCONNECTED
2. - - - — CONNECTIONS FOR OPTIONS.

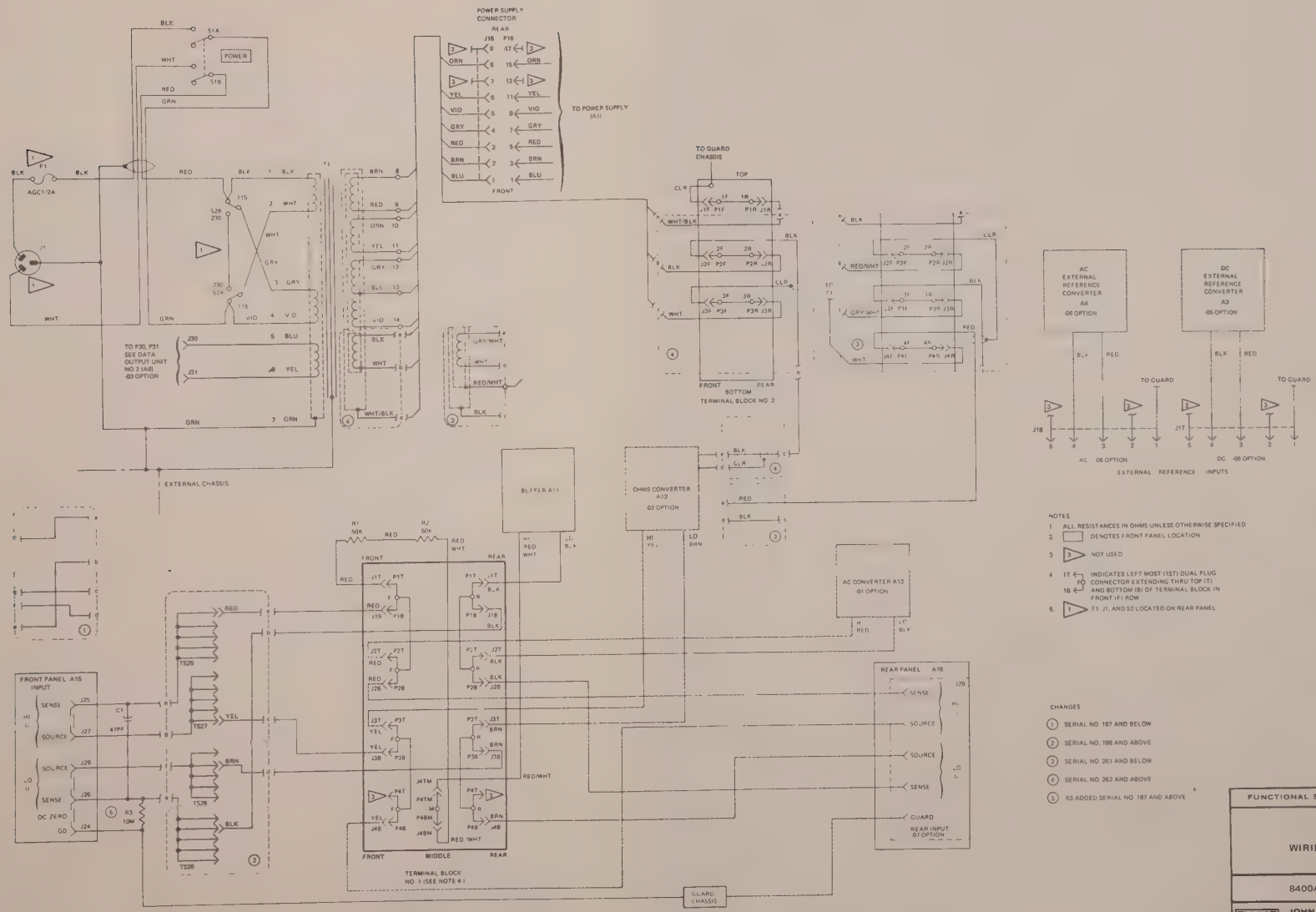
FUNCTIONAL SCHEMATIC DIAGRAM

INTERCONNECT DIAGRAM

8400A-1100

REV —

FLUKE JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle Washington 98133



NOTES

1. ALL RESISTANCES IN OHMS UNLESS OTHERWISE SPECIFIED
2. DENOTES FRONT PANEL LOCATION
3. NOT USED
4. 1T, 1B — INDICATES LEFT MOST (1ST) DUAL PLUG CONNECTOR EXTENDING THRU TOP (T) AND BOTTOM (B) OF TERMINAL BLOCK IN FRONT (F) ROW
5. F1, J1, AND S2 LOCATED ON REAR PANEL

CHANGES

1. SERIAL NO 197 AND BELOW
2. SERIAL NO. 198 AND ABOVE
3. SERIAL NO 261 AND BELOW
4. SERIAL NO 262 AND ABOVE
5. R3 ADDED SERIAL NO 187 AND ABOVE

FUNCTIONAL SCHEMATIC DIAGRAM

WIRING DIAGRAM

8400A-1000 REV b

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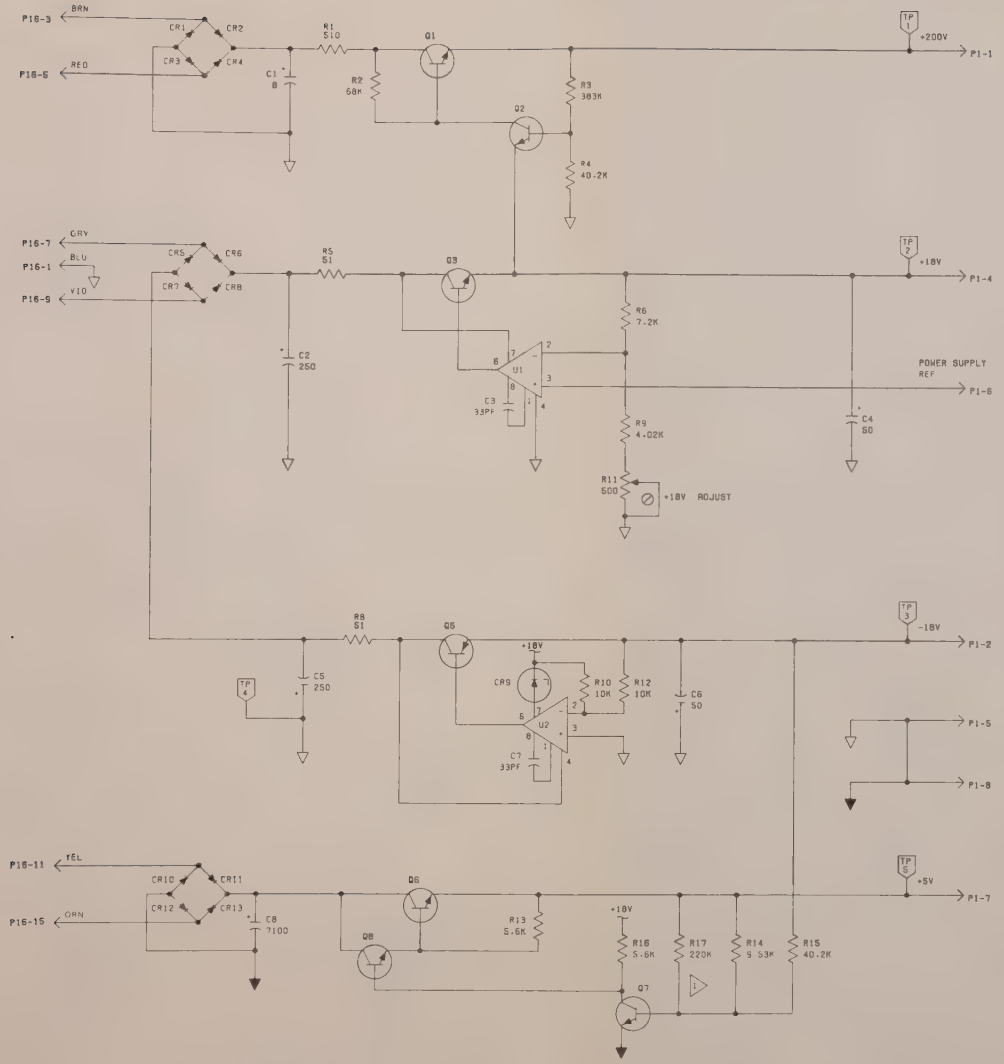

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON.
3. ▼ DENOTES LOGIC COMMON.
4. ⊘ DENOTES INTERNAL ADJUSTMENT.
5. ▷ R17 MAY BE OMITTED DURING ADJUSTMENT OF +5V SUPPLY.

FUNCTIONAL SCHEMATIC DIAGRAM

A1
POWER SUPPLY

8400A-1001 | REV b

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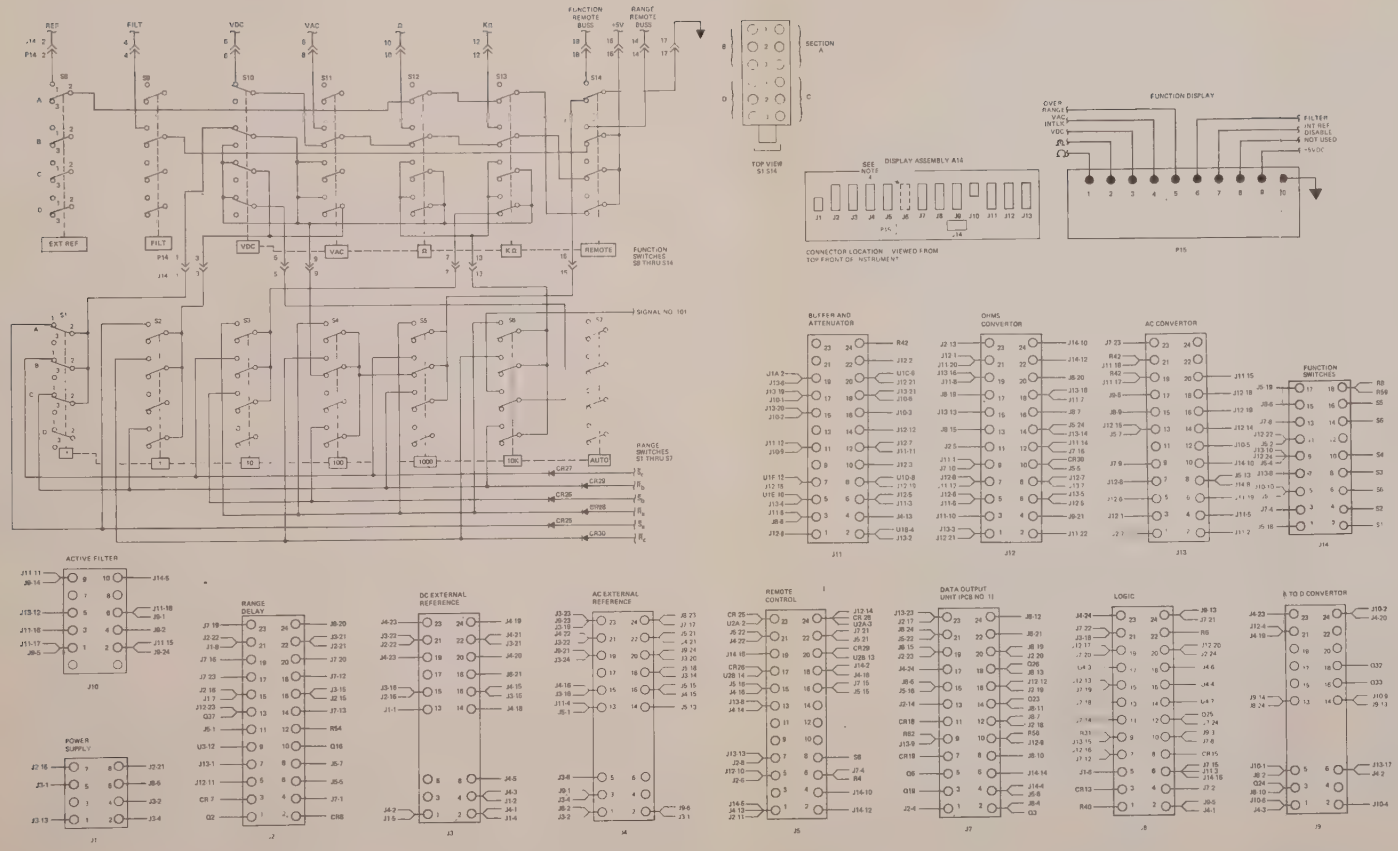
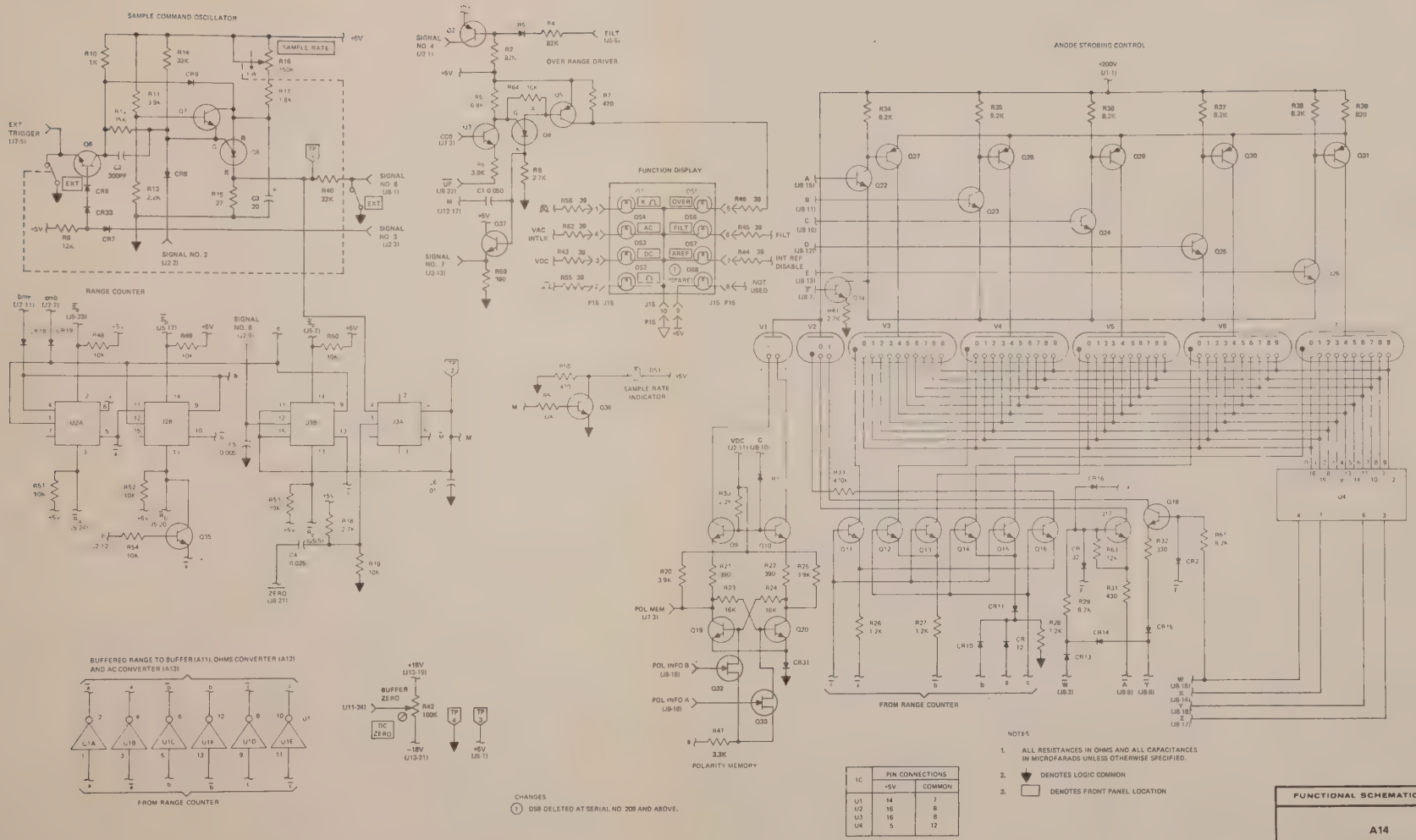


NOTES

1. ▼ DENOTES LOGIC COMMON
2. ▭ DENOTES FRONT PANEL LOCATION
3. CONNECTORS J6, J22, J23, AND J24 MATE WITH P6, P22, P23, AND P24 RESPECTIVELY. IN HARD-WIRED NON-SEPARABLE CONFIGURATION SEE ASS'Y INTERCONNECT DIAGRAM

FUNCTIONAL SCHEMATIC DIAGRAM	
A14 DISPLAY SHEET 1 of 2	
8400A-1002	REV b

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



CHANGES

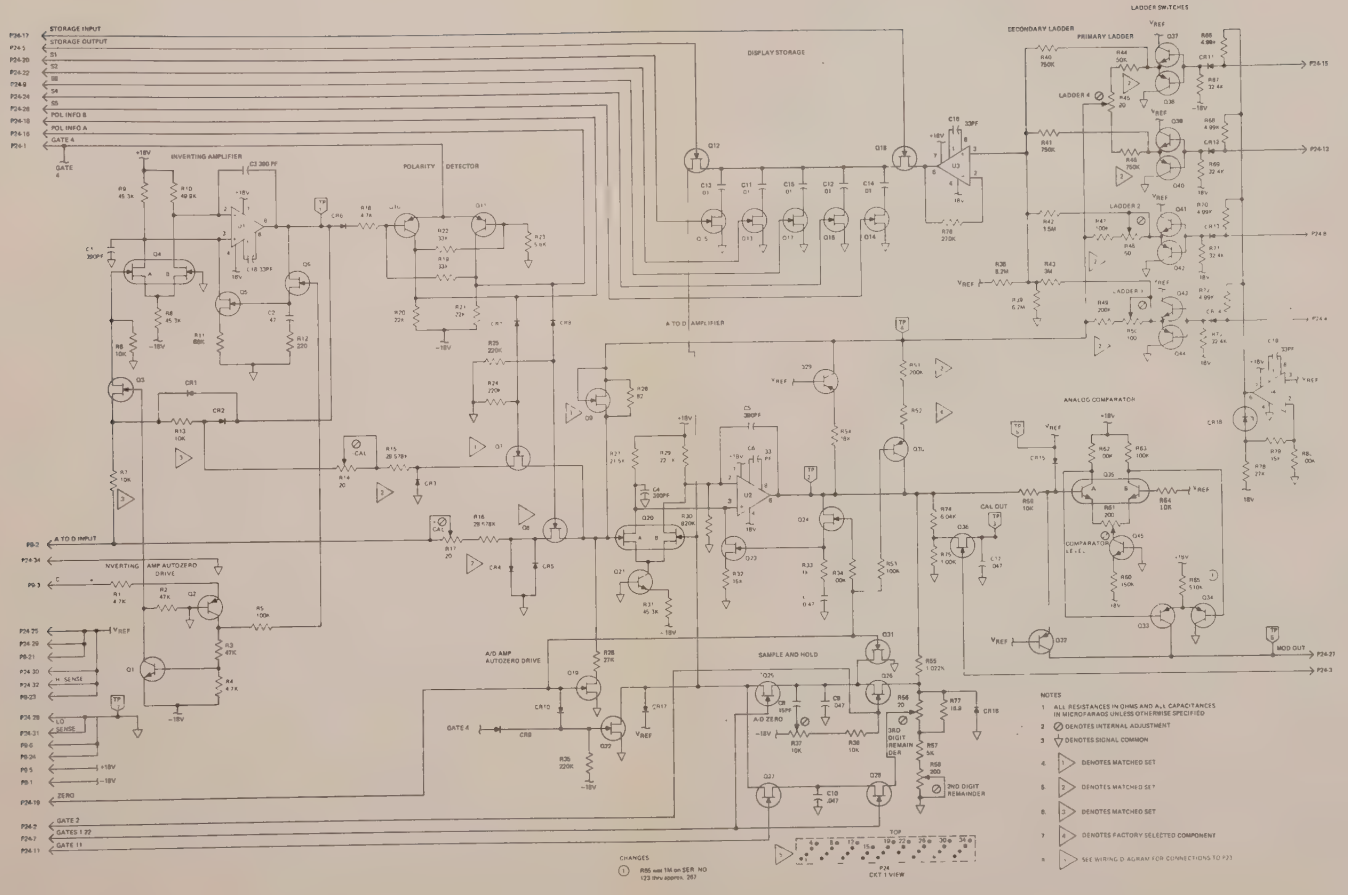
(1) DS8 DELETED AT SERIAL NO. 209 AND ABOVE.

IC	PIN CONNECTIONS	
	+5V	COMMON
U1	14	7
U2	16	8
U3	16	8
U4	5	12

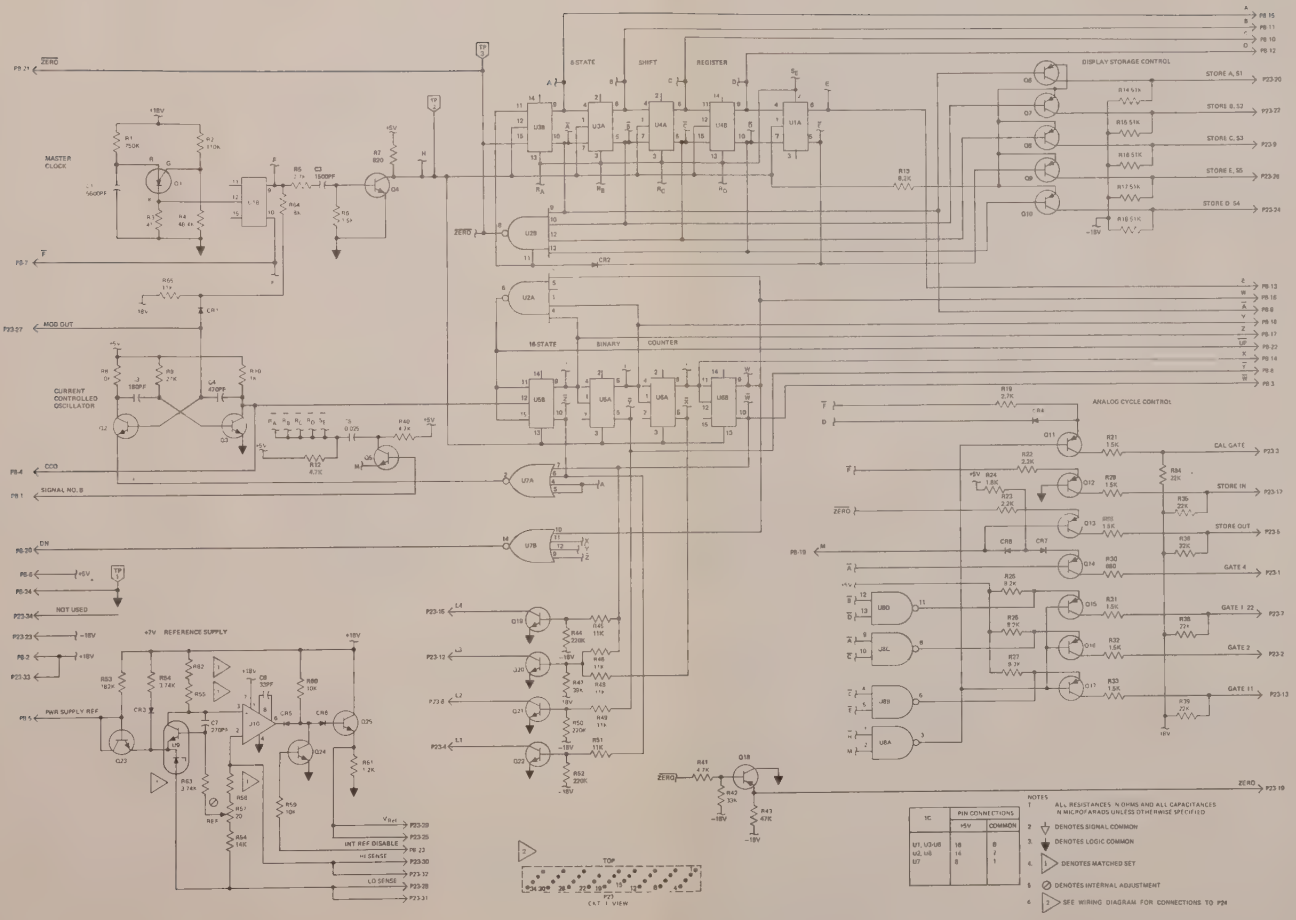
NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ▭ DENOTES FRONT PANEL LOCATION

FUNCTIONAL SCHEMATIC DIAGRAM	
A14	
DISPLAY	
SHEET 2 of 2	
8400A-1002	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



FUNCTIONAL SCHEMATIC DIAGRAM	
A9 A-TO-D CONVERTER	
8400A-1003	REV b
FLUKE JOHN FLUKE MFG CO., INC. P O Box 7428 Seattle Washington 98133	



IC	PIN CONNECTIONS	
	+5V	COMMON
U1, U3-U6, U2, U8, U7	16, 14, 8	8, 7, 1

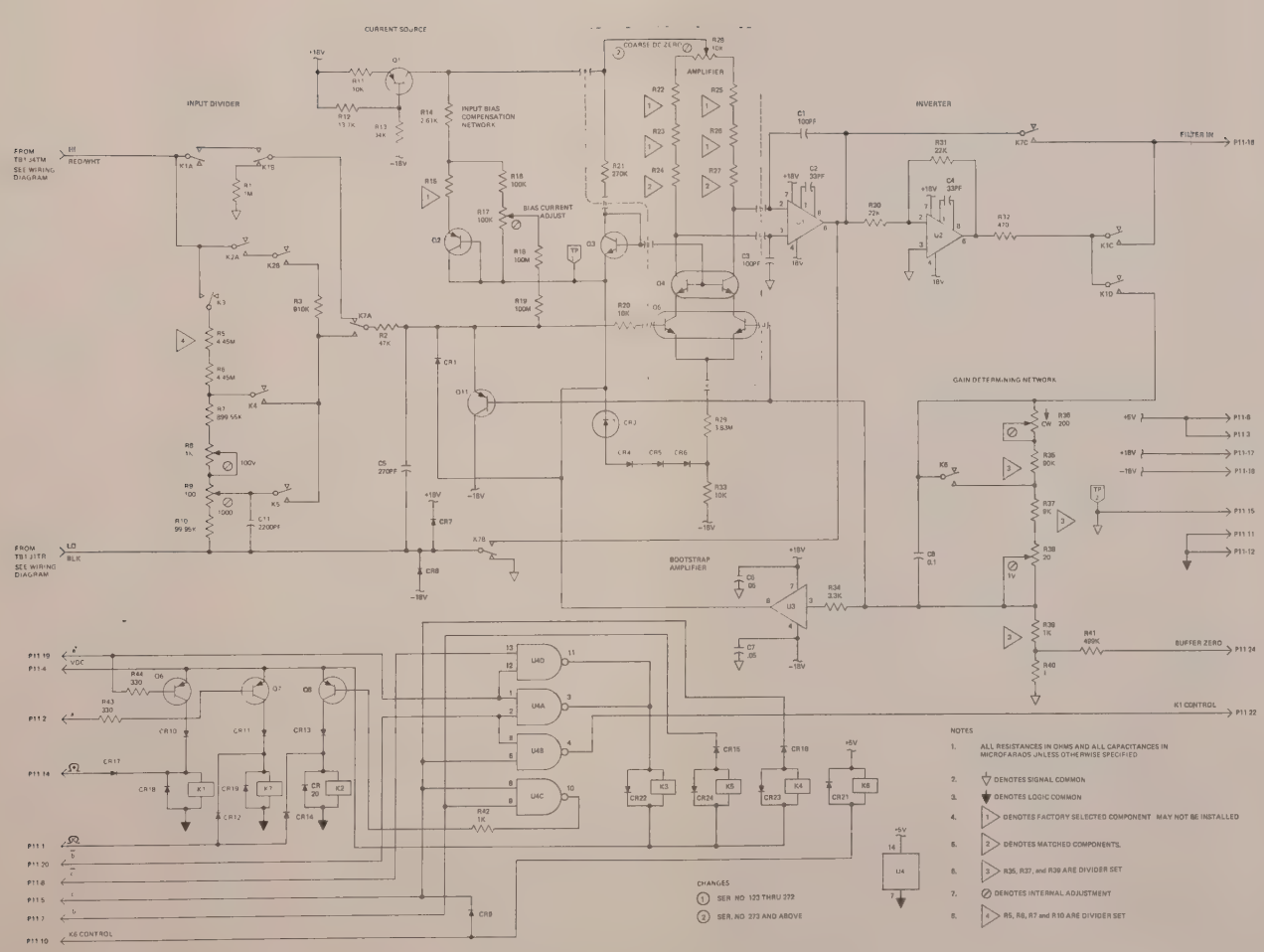
NOTES
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. DENOTES SIGNAL COMMON
3. DENOTES LOGIC COMMON
4. DENOTES MATCHED SET
5. DENOTES INTERNAL ADJUSTMENT
6. SEE WIRING DIAGRAM FOR CONNECTIONS TO P24

FUNCTIONAL SCHEMATIC DIAGRAM

A8
LOGIC

8400A—1004 REV b

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133



BUFFER RELAY LOGIC

	VOLTAGE RANGE				
	LO		HI		
RELAY	0.1	1.0	10	100	1000
K1	*	*			
K2			*		
K3				*	*
K4				*	
K5					*
K6		*			
K7			*	*	*

* INDICATES RELAY ENERGIZED

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ▽ DENOTES SIGNAL COMMON
3. ▼ DENOTES LOGIC COMMON
4. (1) DENOTES FACTORY SELECTED COMPONENT MAY NOT BE INSTALLED
5. (2) DENOTES MATCHED COMPONENTS.
6. (3) R35, R37, and R39 ARE DIVIDER SET
7. ⊘ DENOTES INTERNAL ADJUSTMENT
8. (4) R5, R6, R7 and R10 ARE DIVIDER SET

CHANGES

(1) SER NO 123 THRU 272

(2) SER. NO 273 AND ABOVE

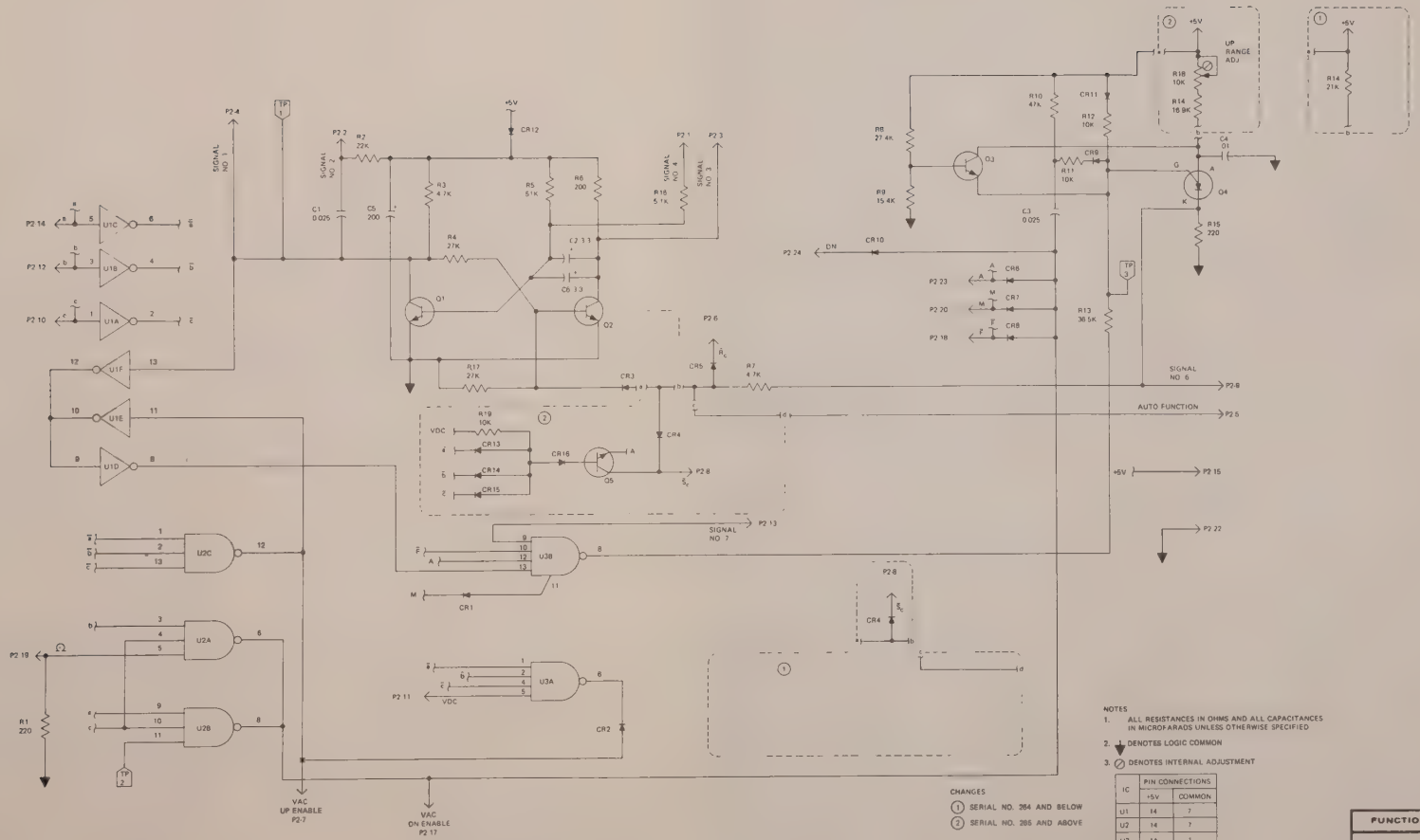
FUNCTIONAL SCHEMATIC DIAGRAM

A11

BUFFER

8400A-1005 REV b

JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle, Washington 98133



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⏚ DENOTES LOGIC COMMON
3. ⊘ DENOTES INTERNAL ADJUSTMENT

IC	PIN CONNECTIONS	
	+5V	COMMON
U1	14	7
U2	14	7
U3	14	7

CHANGES

(1) SERIAL NO. 264 AND BELOW

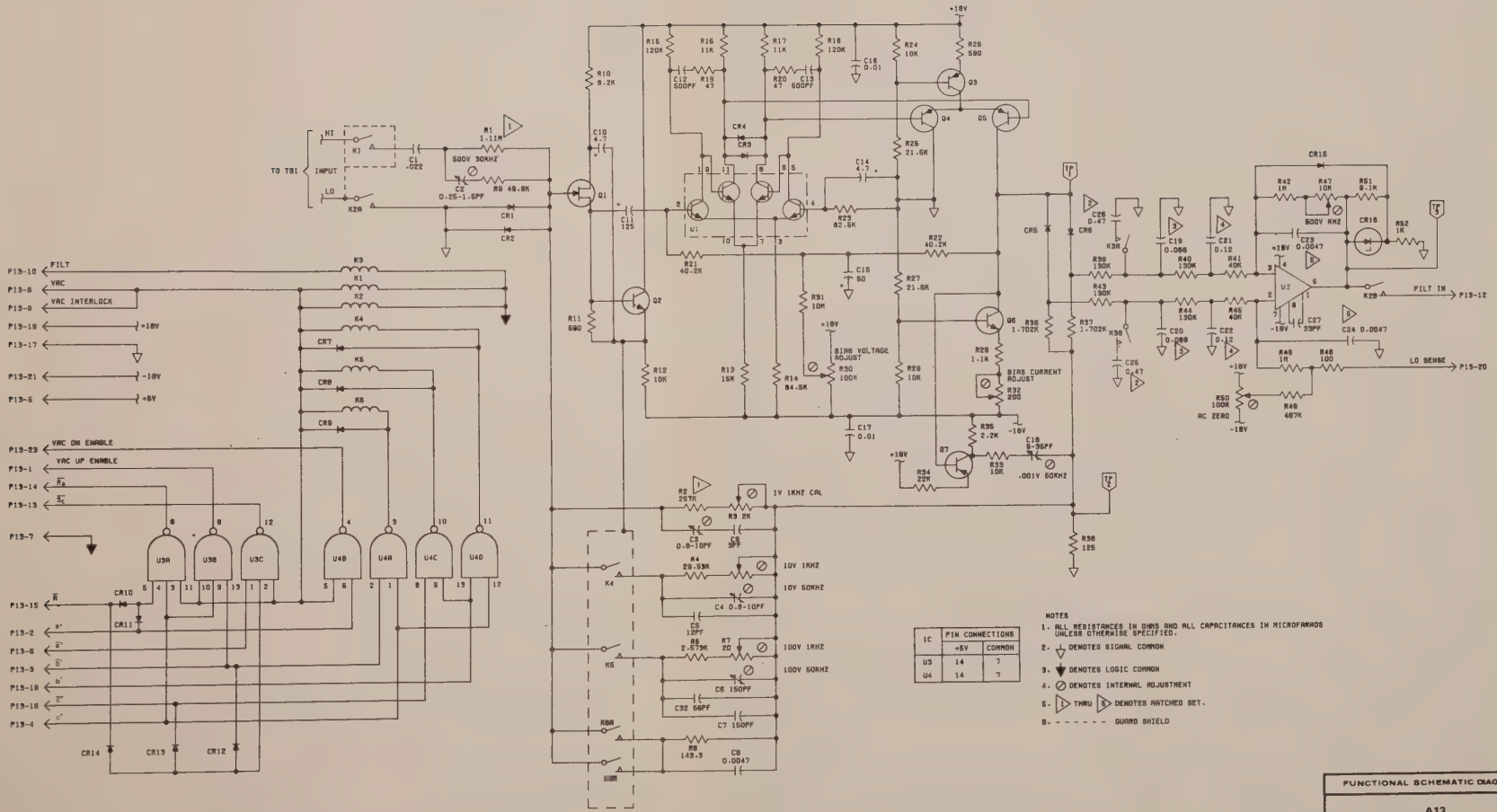
(2) SERIAL NO. 265 AND ABOVE

FUNCTIONAL SCHEMATIC DIAGRAM

A2
RANGE DELAY

8400A–1006 REV b

JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle Washington 98133



IC	PIN CONNECTIONS	
	+5V	COMMON
U3	14	7
U4	14	7

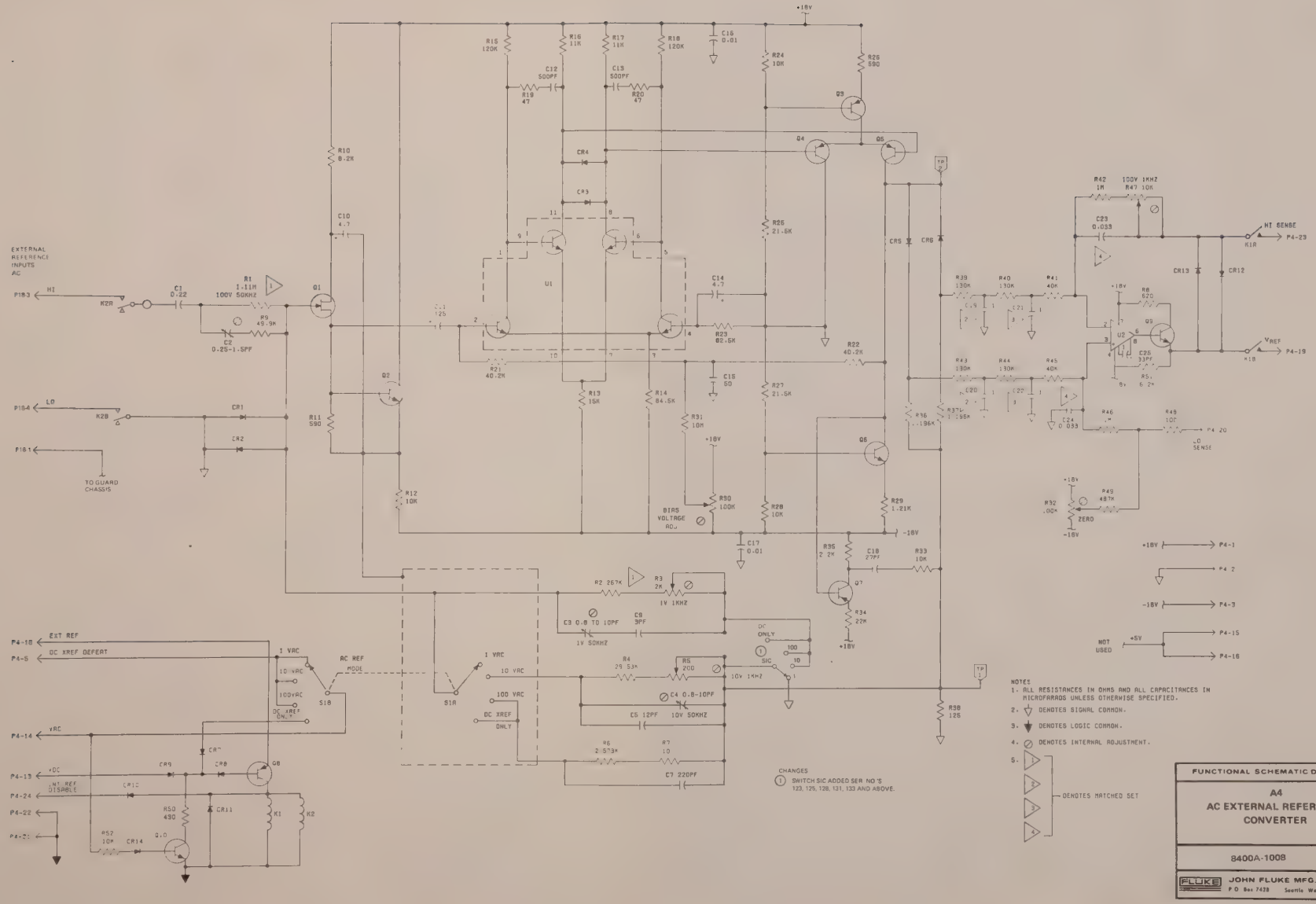
NOTES
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⏚ DENOTES SIGNAL COMMON
3. ▼ DENOTES LOGIC COMMON
4. ⊘ DENOTES INTERNAL ADJUSTMENT
5. (1) THRU (5) DENOTES MATCHED SET.
6. - - - - - - GUARD SHIELD

FUNCTIONAL SCHEMATIC DIAGRAM

A13
AC CONVERTER

8400A—1007 REV b

JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle, Washington 98133

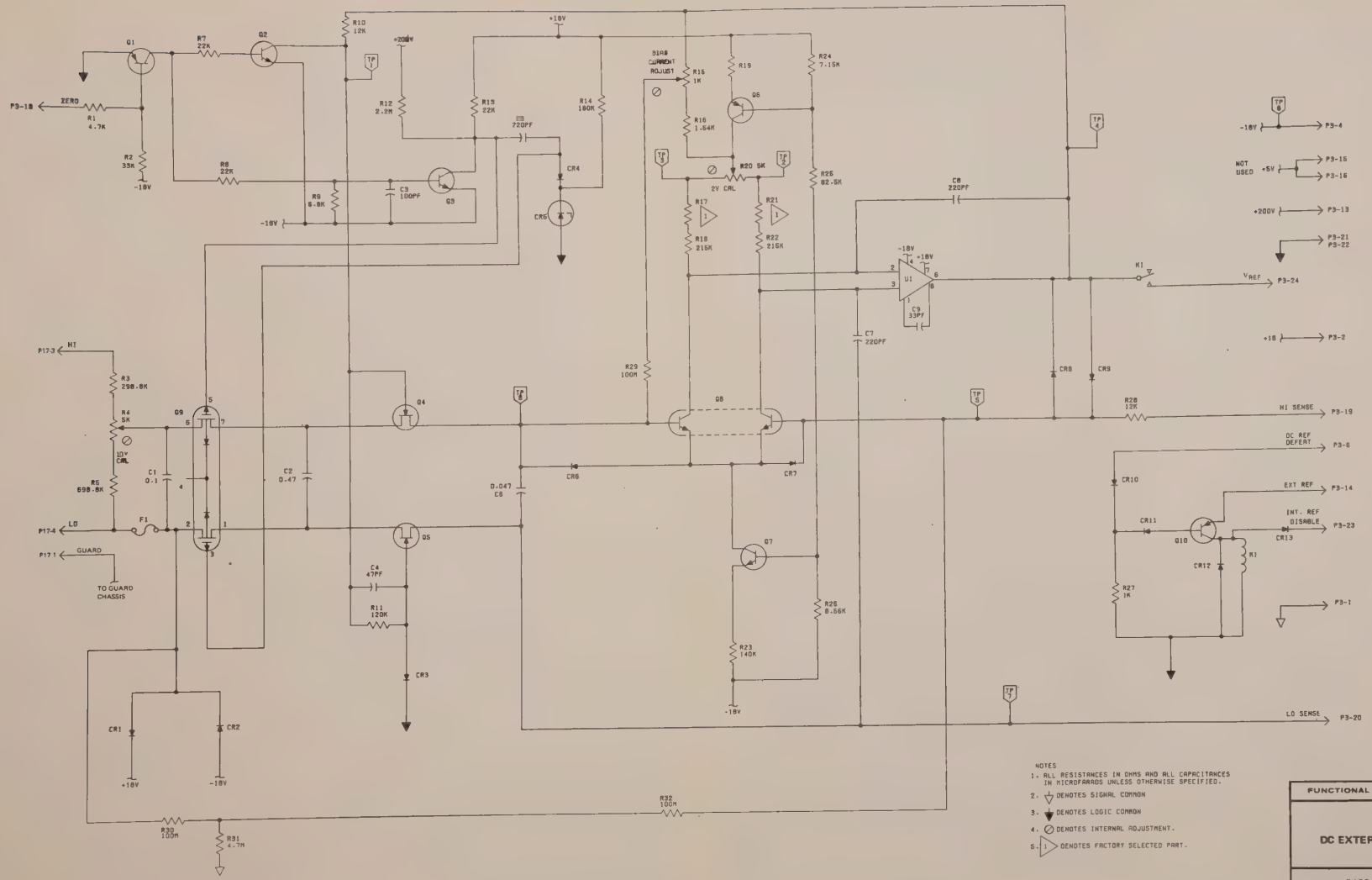


FUNCTIONAL SCHEMATIC DIAGRAM

A4
AC EXTERNAL REFERENCE CONVERTER

8400A-1008 REV b

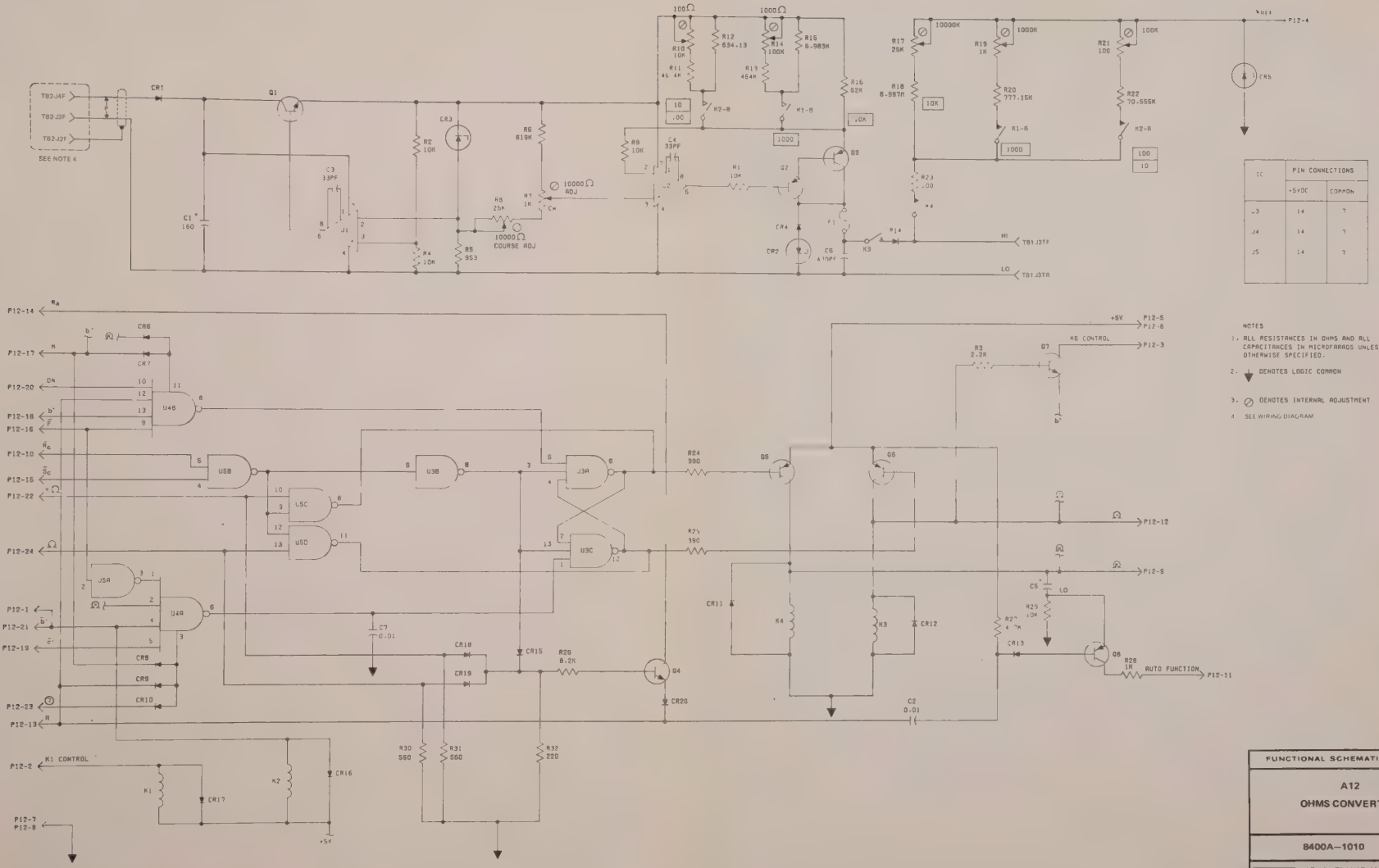
FLUKE JOHN FLUKE MFG. CO., INC
P O Box 7428 Seattle Washington 98133



NOTES
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON
3. ▼ DENOTES LOGIC COMMON
4. ⊘ DENOTES INTERNAL ADJUSTMENT.
5. △1 DENOTES FACTORY SELECTED PART.

FUNCTIONAL SCHEMATIC DIAGRAM	
A3 DC EXTERNAL REFERENCE	
8400A—1009	REV b

FLUKE JOHN FLUKE MFG. CO., INC
P.O. Box 7428 Seattle Washington 98133



NOTES

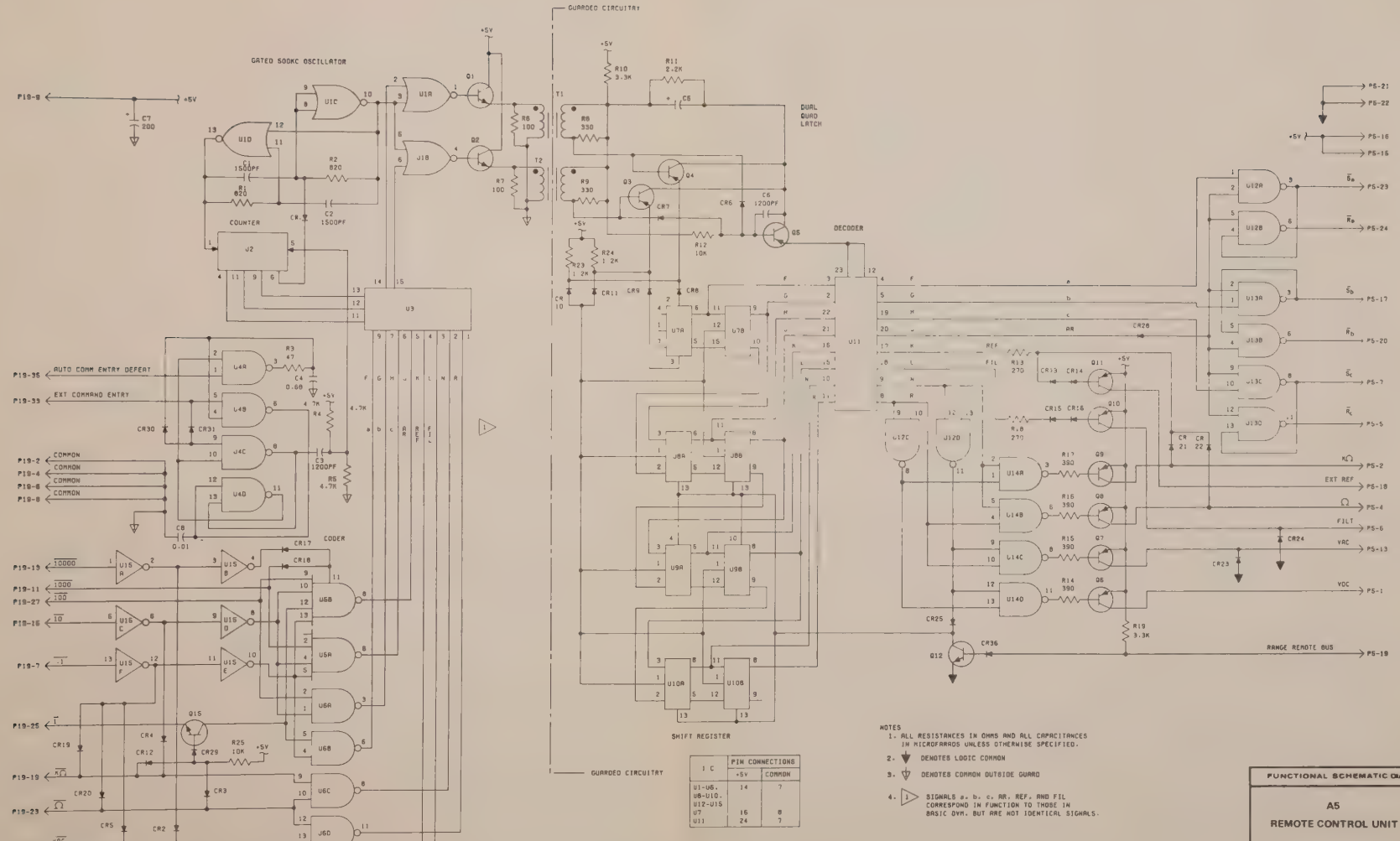
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ⊘ DENOTES INTERNAL ADJUSTMENT
4. SEE WIRING DIAGRAM

FUNCTIONAL SCHEMATIC DIAGRAM

A12
OHMS CONVERTER

8400A–1010 REV b

FLUKE JOHN FLUKE MFG CO., INC.
P.O. Box 7428 Seattle Washington 98133



I C	PIN CONNECTIONS	
	+5V	COMMON
U1-U6, U8-U10, U12-U15	14	7
U7	16	8
U11	24	7

FUNCTIONAL SCHEMATIC DIAGRAM

A5

REMOTE CONTROL UNIT

8400A-1011 REV B

JOHN FLUKE MFG. CO., INC.
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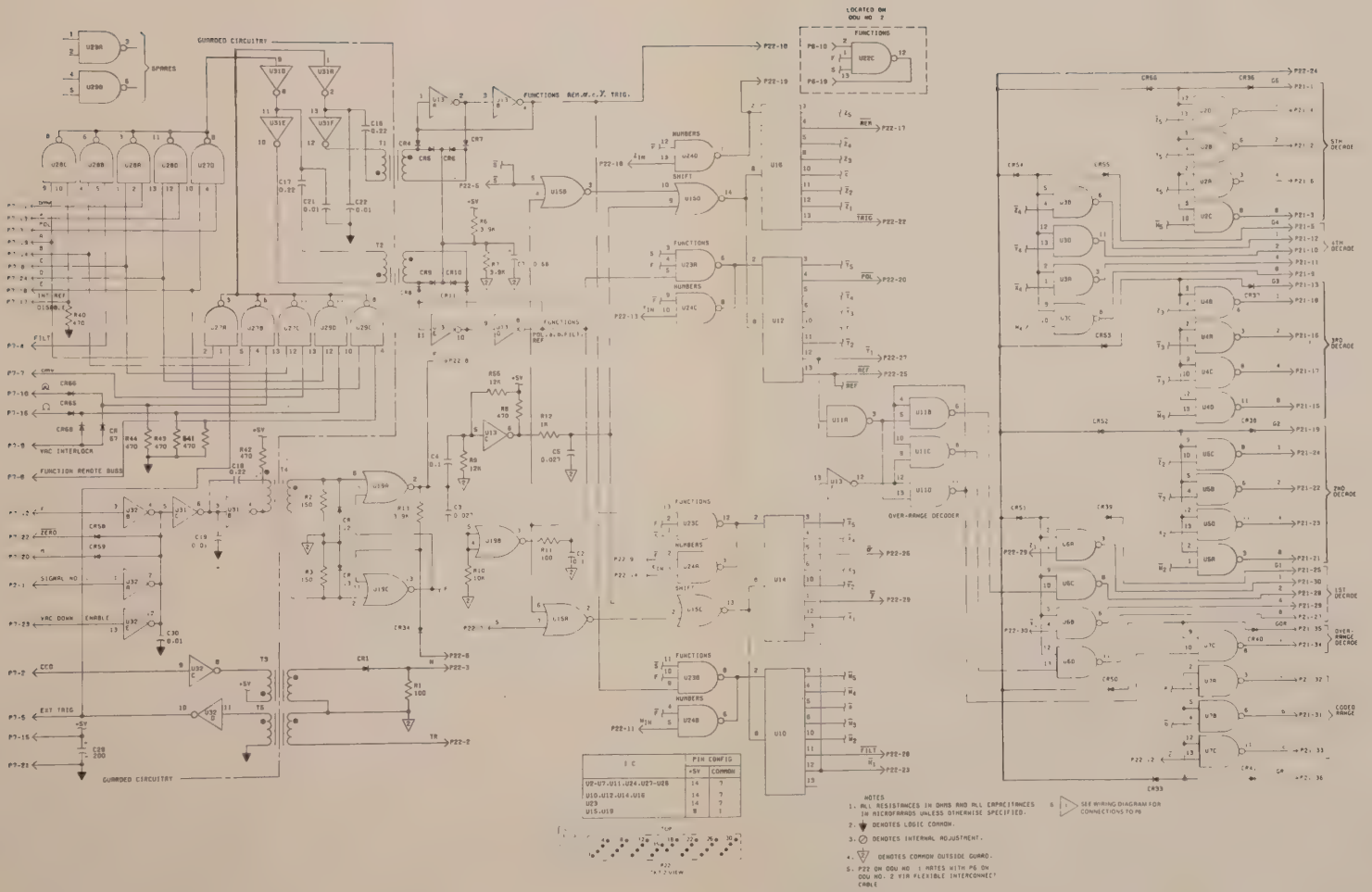


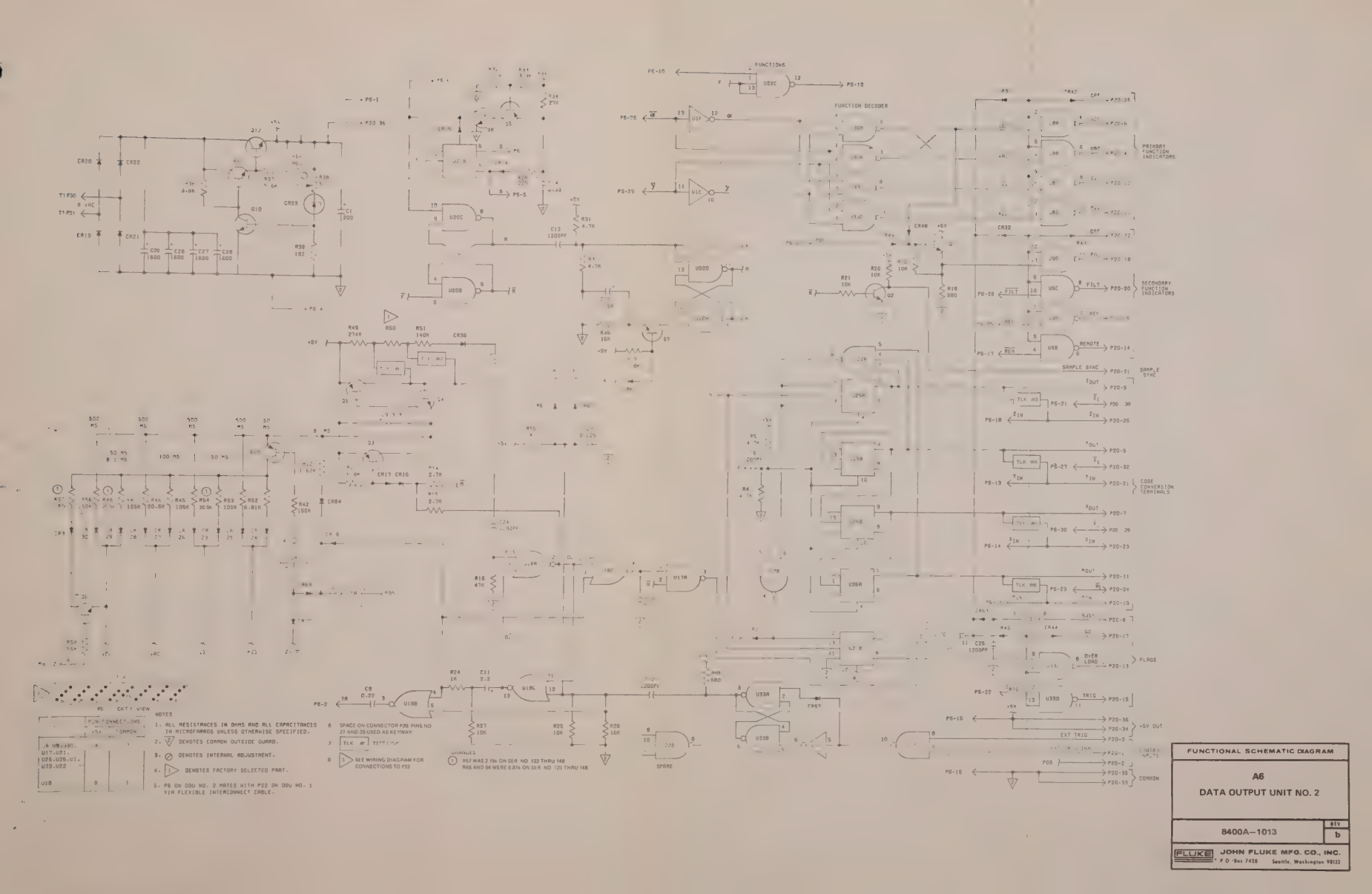
I C	PIN CONFIG	
	+5V	COMMON
U2-U7, U11, U24, U27-U28	14	7
U10, U12, U14, U16	14	7
U23	14	7
U15, U19	8	1

FUNCTIONAL SCHEMATIC DIAGRAM

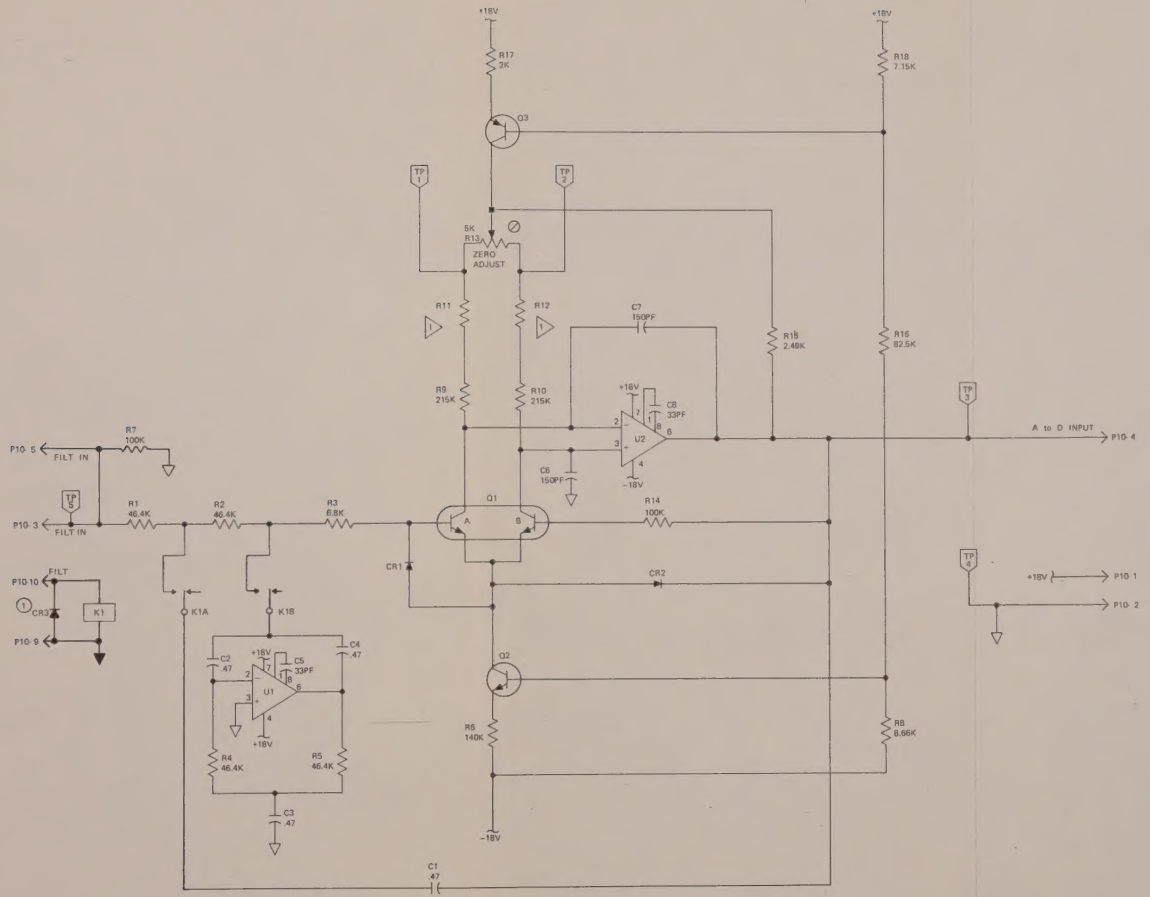
A7
DATA OUTPUT UNIT NO. 1

8400A-1012 REV C

JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle Washington 98133



FUNCTIONAL SCHEMATIC DIAGRAM	
A6 DATA OUTPUT UNIT NO. 2	
8400A–1013	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	



CHANGES

(1) CR3 ADDED AT SERIAL NO. 198 AND ABOVE

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON.
3. ▼ DENOTES LOGIC COMMON.
4. ▷ FACTORY SELECTED
5. ⊘ DENOTES INTERNAL ADJUSTMENT

FUNCTIONAL SCHEMATIC DIAGRAM	
A10 ACTIVE FILTER	
8400A-1015	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

4-10-72

LITHO U.S.A.

FLUKE®

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